Low Temperature Thermal Cycle Survivability and Reliability Study for Brushless Motor Drive Electronics

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Abstract—[1,2] This paper presents a survivability and reliability investigation for integrated actuator and brushless motor drive electronics packaging and components under an extreme low temperature and high thermal cycle environment. A universal brushless motor drive electronics assembly has been designed, built, and thermal cycle tested for use in Mars, moon, and asteroid type cold environments without the need for any active thermal control. The assembly uses electronic part types and chip-on-board electronic packaging technology that allow operation at temperatures down to –180°C. The thermal cycle capability of the assembly has been demonstrated to be in excess of 2010 cycles from -120°C to 85°C, over a 210°C total temperature swing. Future space missions will require electronic and actuator systems on a planet, asteroid or moon surface to function beyond the established reliability limits of currently used components and materials systems. In support of this target application, the Jet Propulsion Laboratory (JPL) has performed a series of experiments to test the reliability of actuators, sensors, electronic components, and electronic packaging designs to provide input to the detailed flight design of a universal brushless motor drive electronics and integrated actuator assembly. These experiments started with the use of a chip-on-board electronic packaging strategy due to its inherent advantage of improved high functionality with minimal circuit board area compared with standard packaged electronic components. Initial electronic packaging experiments were comprised of various sized chip devices with gold wire bonds. The second phase of electronic packaging experiments conducted at JPL consisted of power devices with large diameter wire bonds as well as various surface mount resistor devices. Full factorial experiments were designed to find the most reliable combinations of substrate type, component attach method and encapsulation. The surviving material combinations after a minimum of 1500 thermal cycles were utilized to form the basis of the packaging and electronic component detailed design approach used in the universal brushless motor drive electronics design. Electrical failures were defined as open circuits. A failure analysis procedure was applied by defining the failure mechanism and applying a risk mitigation. After 1500 cycles, the packaged assembles were cycled to exceed 2010 cycles and additional material considerations were made. In addition, selected components were functionally tested over the temperature range of +100ºC to -180ºC and cold soaked at -150ºC for 1000 hours for reliability. A design for reliability method was also developed at the component and circuit level for electronics operating at extreme low temperatures.

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1. TARGETED APPLICATIONS

The applications targeted for the fully integrated actuator with drive electronics that can operate below -180°C and survive many large swing thermal cycles include landed missions on airless bodies such as the Moon, asteroids, or comets, landed missions on bodies with atmospheres such as Mars, and all types of orbiter and deep space missions. The extreme low temperature operation capability allows the use of mobility or robotic arm systems with no operational limitations due to the thermal environment.

2. FUNCTIONAL CAPABILITY

The integrated actuator and motor drive electronics form a remote (relative to the system central bus) mechanism driver with the actuator providing mechanical "drive" and the integrated electronics assembly providing electrical "drive". The motor drive electronics have a custom gate array at their core that provides huge functional capability in the complete actuator assembly. The communication interface is composed of a serial bus with no cabling restrictions to connect to it other than shielded twisted pair wires. The drive electronics is capable of driving the motor in many modes including position control, velocity control, current control, stepper, micro-stepping, delta or wye windings, adjustable current limiting, path profiling, open-loop Pulse Width Modulation (PWM), and many others. The drive electronics also interfaces to several analog sensors using any combination of current or voltage stimulation as well as multi-speed resolvers for motor commutation or position or velocity control. Additional capabilities include several local power outputs that can source voltage to items like latches or paraffin actuators, heaters, additional remote sensors, or any other combination that can be imagined.

System mass is reduced in direct proportion to the number of actuators in a flight system by minimizing the cabling requirements and allowing the interconnection of many actuators using the same serial bus cabling. Redundancy is provided in the form of independent power and communication bus inputs. Fault isolation is provided through electronic hardware design or local active switching to isolate any failures and prevent loss of the communication or power busses to the remaining actuator systems.

3. ELECTRONIC PACKAGING OVERVIEW

The electronic packaging task objective was to develop and demonstrate commercially available and space qualifiable electronic packaging technology that would enable electronics assemblies to survive 670 thermal cycles in the Mars ambient environment (-120°C to +20°C) with an electronics functional range of -120°C to +85°C. For qualification, a life test margin of 3X is applied, resulting in a survival requirement of 2010 thermal cycles from -120°C to +85°C. The design is modular in nature, allowing the drive electronics and actuator to be integrated prior to Spacecraft System Assembly, leaving only a communication interface for integration at the system level. The modular design enables the actuator controller to have application for all future space and landed missions.

The commercial state of the art for electronics packaging is the Mil-Spec electronics, rated for –55 to +125°C operation, and typically for a few hundred temperature cycles. The Sojourner rover and the two Mars Exploration Rovers employ active thermal control (i.e., a warm electronic box, or WEB) in combination with a centralized electronics architecture to maintain the electronics within acceptable temperature limits. This approach imposes a serious penalty in terms of cabling design complexity and magnitude of wiring (many hundreds or thousands of wires) used to connect key sensors, instruments, and actuators to the centralized core computer system. Other penalties include the challenging thermal design required due to the thermal leaks into and out of the WEB created by the large quantity of wires.

The mechanical packaging architecture incorporates polyimide rigid-flex technology configured into a significantly smaller volume, 262.2cm^3 and mass, 300gm, than the standard centralized controller. The relative reductions are 10X in volume and 3X in mass. The integrated actuator and electronics approach distributes the power switching and actuator control to the location at which the mechanical output is required, creating a distributed control system.

The heart of the packaging approach makes use of a high density mix of two sided SMT (surface mount technology) and two sided COB (chip-on-board) methods. The small size and integrated design mixes high precision low voltage signals with digital control signals as well as high current, high switching frequency power. Due to the increased JPL technical capabilities created by this approach, a California Institute of Technology Provisional Patent (case no: NPO41776) has been awarded.

The motor drive electronics assembly is composed of 1100+ electronics parts (250 are bare die) with aluminum and gold wire bonds on a high density 2-sided rigid-flex polyimide

printed wiring board that folds into a 76.2mm cube.

The development effort was composed of building representative Test Vehicle units for parametric testing of various material combinations over the large temperature range. Testing performed by the Thermal Cycle Resistant Electronics (TCRE) technology development program has shown that a high density mix of SMT and COB can survive and operate under the extreme Martian temperatures along with the understanding of how to manufacture and handle the selected technologies.

The modular design of the drive electronics requires handling a high number of external connections in order to provide the application flexibility needed for the universal nature of the electronic drive assembly. This allows all mechanism drive functions to interface only with the actuator drive electronics, eliminating additional system cabling for those functions. This has driven the need to handle over 150 external I/Os and 3800 internal interconnects. Power densities range from 8 watts/ $262.2cm^3$ at steady state and 46.3 watts/ $262.2cm^3$ peak power. The development of the universal motor drive electronics assembly has extended JPLs design capabilities, allowing for significant improvement in system packaging architecture options.

4. THERMAL CYCLE RESISTANT ELECTRONICS (TCRE) BACKGROUND

The Jet Propulsion Laboratory as part of the Mars Technology program has been tasked to develop electronic components and electronics packaging technology that is capable of operating in the ambient temperature of Mars without any thermal control. This technology development program, called Thermal Cycle Resistant Electronics (TCRE), is a design for reliability activity.
The Thermal Cycle Resistant Electronics (TCRE) technology development program is divided into two parts, the electronics and packaging. This program has an objective of developing packaging assemblies that must survive in the Mars ambient environment (-120ºC to +20ºC), and developing electronic components for a temperature range of -120ºC to +85ºC with required long term reliability target.

The electronics task investigates the performance of commercial off the shelf (COTS) as a function of temperature. Since COTS are designed for terrestrial applications (-55ºC to 110ºC), they may fail to function at Mars temperatures. Hence their performance and life cycle under Mars environment has to be characterized. Focusing on the COTS needed for developing an integrated motor controller module TCRE electronics has: 1) developed a candidate list of COTS, 2) Characterized the COTS as a function of temperatures and 3) Validated their life cycle.

TCRE electronics task has also developed a rad tolerant wide temperature quad operational amplifier for the Mars environment. This is because commercially available operational amplifiers failed to provide performance needed for sense and control of analog signals in the motor drive electronics. The quad operational amplifier has been developed on the Honeywell 0.35µm electronics space rated Silicon-On-Insulator CMOS (SOICMOS) technology with special design rules that enhances the performance and life of the operational amplifier under low temperatures of Mars. JPL has developed the design rules by examining the reliability of individual transistors in the SOI CMOS technology at low temperatures and modeled the life of the transistors as a function of its geometric parameters (transistor channel width and length). To minimize the developmental costs, the quad operational amplifier was initially prototyped and functionally verified on the commercial Honeywell SOI CMOS fabrication line. It was then ported to the more expensive space rated and rad tolerant version of the CMOS technology. The amplifier is now base lined for use in the MSL rover.

The TCRE packaging develops a reliable, low-temperature packaging technology, that can survive thermal cycling from -120ºC to 85ºC. Material properties, such as modulus of elasticity and thermal coefficient of expansion, of these packaging materials are not known at low temperatures. The continuous change of temperature in the Mars environment introduces electronic reliability factors that are due to thermally induced fatigue of the IC package.

To support the development of a reliable cycle resistant packaging technology, TCRE developed electronic assemblies and selected a combination of substrate, die attach, and encapsulant materials, that can survive for an extended mission in a Mars environment. These electronic assemblies consisted of surface mount components such as bare die with wire bonds, and passive and active devices. A full factorial experiment and large sample size was formed in order to ensure a statistical confidence. A large sample size was also needed because of the dearth amount of material property data known at low temperatures. All packaged assemblies were thermal cycled from -120°C to 85°C in excess of 2010 cycles. Continuous and manual functionality measurements were taken throughout the duration of cycling in order to find electrical failures. Failure analysis was applied, the root cause was established, and the risk mitigation was tested. Surviving material combinations, design, and assembly processes were implemented into the EDU1 for the motor drive electronics.

5. TCRE PACKAGING EXPERIMENTAL DETAILS

The first of the test vehicles was called TV1 or Test Vehicle (TV) 1. This TV1 experiment began the extensive materials selection process and tested the survivability of a silicon die mounted to a substrate with gold wire bond electrical interconnects [1]. From that experiment, the surviving material combinations were implemented onto Test Vehicle 2 (TV2). The TV2 experiment was composed of several surface mount electronic components from the universal motor drive electronics design.

5.1 Test Vehicle Design

The circuitry of the test vehicle was designed on polyimide and ceramic substrates. Each polyimide and ceramic substrate had a thickness of 1.60mm +/- 0.127mm and was approximately 51.69mm by 47.75mm.

TV1 and TV2 polyimide substrates were composed of 2 and 8 layers, respectively. The polyimide substrates had wire bondable Au plating (1.016-1.524μm) at 99.97% purity with a Ni underplate (2.54 – 5.08μm) per SAE-AMS-QQ-N-290 Class 2. The TV1 substrates had a top layer of Cu at 35.7μm. The TV2 substrates had a top layer of Cu at ~107 μm thickness. A LPI solder mask was included on both TV1 and TV2.

The thick-film alumina (96% minimum aluminum oxide, as fired) and LTCC (LTCC Ferro A6 with 93.98μm thick laminate minimum on TV1 and Dupont Green Tape 95 with 96.52 μm minimum fired thickness on TV2) substrates were composed of two (TV1) and four (TV2) thick-film and backside metallization layers. Both TV1 and TV2 alumina substrates had a Dupont Fritless Au 5715 metallization layer for soldering and a double print of a Dupont Pt/Pd Au 4596 for wire bonding. On the TV1 LTCC substrate, the metallization layer for soldering was a thick-film Au, Kyrocera 30-065VM2 conductor with a purity of at least 99.99%. A thick-film, Dupont Pt/Pd Au 4596 was used for wire bonding. On the TV2 LTCC substrate, the metallization layer for soldering was a thick-film Dupont Pt/Au 5739. A thick-film Dupont Au 5734 was used for wire bonding.

All through-hole vias on the TV1 and TV2 substrates had a diameter of 508 μm +/- 50.8 μm. The vias on polyimide were plated with a minimum Cu thickness of 25.4 μm. The vias on thick-film alumina were filled with Dupont Au 9591 or 5727. The vias on LTCC were filled with thick-film Au, Kyrocera 30-065VM2 with a purity of at least 99.99% on TV1 and thick-film Au 5738 on TV2.

The TV1 test vehicle had a pad layout to accommodate the silicon die. The substrate top side consisted of three gold finished pads that are sized to have a die that is 10mm x 10 mm, 5mm x 5mm and 2.2mm x 2.2mm placed on them. Each TV substrate contained thirteen individual conductive circuits. The circuits were made up of three different types; 7 were for strain gauges, 4 were for daisy chains and 2 were for via chains. In addition, there were 2 electrical circuits that ran through traces on both sides of the substrate through 58 through-hole vias on the outer side edges of the substrate.

The 10mm x 10mm and the 5mm x 5mm silicon die had aluminum pads around the perimeter that were provided to allow a daisy chain of wire bonds from the substrate to the die and back multiple times for building a continuous circuit. In addition, each die was fabricated with a strain gage circuit, two per quadrant and eight per die. The 2.2mm x 2.2mm die was fabricated with only pads for building a continuous circuit and did not contain any strain gage circuitry. Figure 1 shows an example of a 5 mm die and the electrical traces that run to it and contain one continuous electrical path daisy chained.
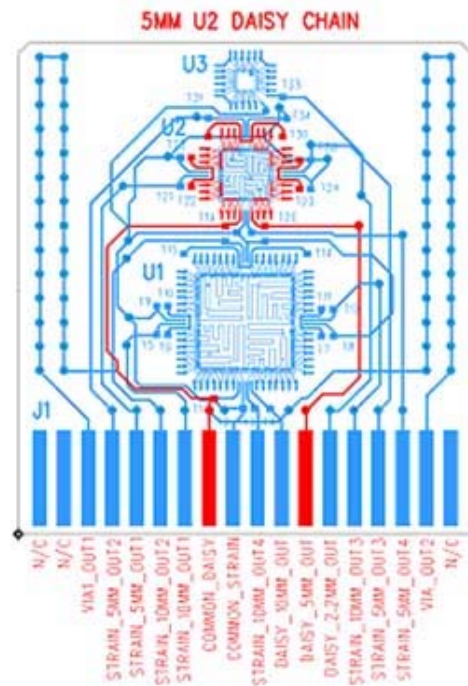

Figure 1: 5 mm die with daisy chain circuit around the perimeter

The bottom portion of the substrate contained one large gold plated pad 22mm x 22mm that was provided as a mounting location for a bare silicon die and was not electrically connected to any continuity circuit. The purpose of this die was to observe its mechanical attachment during thermal cycling. The pad on the bottom side of the substrate was fabricated at JPL and cut to 22mm x 22mm. It had no trace or pad metallization on its top surface.

The TV2 test vehicle had a pad layout to accommodate several surface mount components: 37- pin Nanonics Dualobe® connector (nano-connector) with surface mount BeCu leads and a standard Sn60Pb40 finish over a Cu strike per SAE-AMS-C-81728, two International Rectifier (IR) power MOSFETs (IRHC57260SECDV) with 508μm diameter wire bonds to the source pads and 127μm diameter heavy aluminum (Al) wire bonds to the gate pad, and four discrete surface mount resistors. R1 resistor at 1000 Ohms with a 1206 package size had either Ni/Au or Sn90Pb10 endcap finish. R2 resistor at 100 Ohms with a 0805 package size also had the same endcap finishes as R1. The R3 resistor at 100 Ohms with a 1506 package size had a SnPbAg finish. The R4 resistor at 100 Ohms with a 1506 package size had either a Ni/Au or Sn62Pb36Ag2 finish. Through-hole and buried vias were designed onto the polyimide boards.

The substrates contained traces that connected each component into one continuous electrical circuit. The 37 nano-connector lead pads and through-hole and buried vias were daisy chained independently into one complete circuit as shown in Figure 2. All four heavy Al wire bond source pads on both MOSFETS were daisy chained with jumper wire bonds in order to complete the circuit between both die.
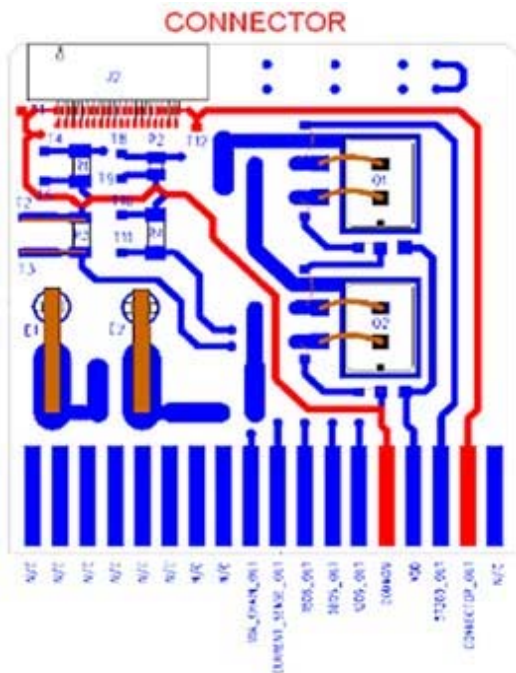

Figure 2: Connector daisy chained circuit

5.2 .Materials Selection

The TV1 substrate, die attach, encapsulant, and wire bond materials are shown in Table 1. Each material was chosen based on the following criteria.

Polyimide was selected as it has the best properties for an organic and is the most common space flight circuit board material. Alumina was selected because of its military and space heritage for use in hybrid circuits as well as superior expansion and toughness characteristics. LTCC was selected as having good expansion properties as well as ease of incorporating multilayer design, which is likely to be required.

For die attach materials, the team's initial decision was to select a candidate material from each of the major material categories, therefore, an epoxy, a silicone and a solder were selected. The vendor recommended two flexible epoxy materials, Ablebond 976-1 and Ablebond 967-1. Ablebond 967-1 was selected due to its lower glass transition temperature of 75°C. Silicones were considered because of their very low Tg and high compliance. The Dow-Corning material HIPEC Q1-4939 was recommended by APL based on their experience.

There are several reasons for using an encapsulant or overcoat on Chip-On-Board assemblies. The encapsulant provides a barrier to protect the circuitry from moisture and other contaminates. In addition, an encapsulant or overcoat can provide mechanical or structural protection to the delicate active circuitry and wire bonds during handling and service life.

Representative encapsulant and coating materials from three different categories were chosen. An epoxy (FP-4402) a silicone (HIPEC Q1-4939) and Parylene-C. The first two materials are considered "glob-top" materials encapsulating the entire COB sub-assembly and the third is a thin coating. The epoxy has an extensive military and space flight heritage, the silicone was selected for its compliance properties. The advantage of using Q1-4939 as an encapsulant includes a good moisture barrier and it also provides some mechanical protection. It should be noted that this mechanical protection would only be adequate against very small forces that are in the 5 to 10 gram range or less; this is based on speculation from handling experience and not on any controlled measurement testing. The advantages of using FP-4402 as an encapsulant include very good moisture protection and superior mechanical protection. Parylene C also has space flight heritage and is considered a very low stress material. The advantages of Parylene-C coated assemblies include low stress, high compliance and a uniform and accurate coating thickness that provides very good moisture protection.

	Materials Matrix
	Table 1: TV1: Materials Matrix
Substrate	Polyimide, Alumina (Al2O3), Low Temperature Co-Fired Ceramic (LTCC)
Die Attach	Pure Indium, Silver Filled Epoxy(Ablebond 967-1), Silicone Based Adhesive (Zymet

	TC-611)	
Encapsulant	Epoxy(Hysol FP-4402), Silicone Based(Dow Q1-4939), Parylene C	
Wire	99.9% Au .001" in diameter	

The surviving material combinations from TV1 were implemented onto TV2. The conformal coatings, Dow Q1 4939 1:10 ratio, and Parylene C, and die attach materials, Ablebond 967-1, Zymet TC-611 were included. New materials, In80Pb15Ag5 solder (Indalloy #2- Indium Corporation of America), Sn63Pb37 eutectic solder, an additional silicone based adhesive, (Zymet 6000.2, electrically and thermally conductive adhesive), and 2216 B/A (3M Scotch-Weld epoxy), were implemented. In80Pb15Ag5 solder was selected because of its thermal fatigue resistance and minimized leaching when soldering to Au.[3] All TV2 materials are defined in Table 2.

Table 2: TV2 Packaging Material Selection

	Materials Matrix
MOSFET Die	Silver Filled Epoxy (Ablebond 967-1); Indium solder alloy (In80Pb15Ag5;); Silicone Based Adhesive (Zymet 6000.2)
Surface Mount Resistors	Silver Filled Epoxy (Ablebond 967-1) Indium solder alloy (In80Pb15Ag5); Silicone Based Adhesive Staking for R3 (Zymet TC-611)
Nano-connector Leads	Indium solder alloy (In80Pb15Ag5); Eutectic solder (Sn63Pb37)
Nano-connector Aluminum Shell	Epoxy (2216 B/A); Silicone Based Adhesive (Zymet TC-611)
Conformal Coating	Silicone Based (Dow Q1-4939), Parylene C
Substrate	thick-film alumina (96% minimum aluminum oxide), Low Temperature Co-fired Ceramic (LTCC) and polyimide (epoxy resin based) each with identical circuitry.
Wire	99.999% Al 508μm in diameter 99.99% Al 127μm in diameter 32 awg (Ag plated Cu wire)

5.3.Test Vehicle Assembly Processes

Both TV1 and TV2 were assembled according to the following procedures.

The TV1's were cleaned prior to assembly. The polyimide substrates were cleaned with a solvent and the alumina and LTCC substrates were plasma cleaned. The Ablebond 967-1 silver filled epoxy and the Zymet TC-611 was stencil printed onto the substrates prior to die placement. After placement the adhesive was cured. The pure Indium was applied as a perform-76.2μm thick. Flux was applied to the substrate and the die. The preform was reflowed on a hot plate at 180°C. All substrates to die electrical connections were completed with 25.4μm diameter pure gold wire (99.99%). The connection at the die interface was a ball bond and the connection at the substrate was a wedge bond. Pull tests were performed on a sample substrate with each wire bond setup. The application of the encapsulant or conformal coatings was the final step. The Hysol FP-4402 epoxy was dispensed over the die on each substrate and cured. The Dow Q1-4939 was also dispensed over the dice on each substrate per the DOE matrix and cured. The Parylene C was vapor deposited over the entire test vehicle assembly (less the masked coupon edge connector pads) in a vacuum chamber to a thickness of 25.4μm per the DOE

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[3]Master Solder Alloy Properties Table, from the Indium Corp.website<http://www.indium.com/products/oldalloychart.php> accessed November 2, 2004

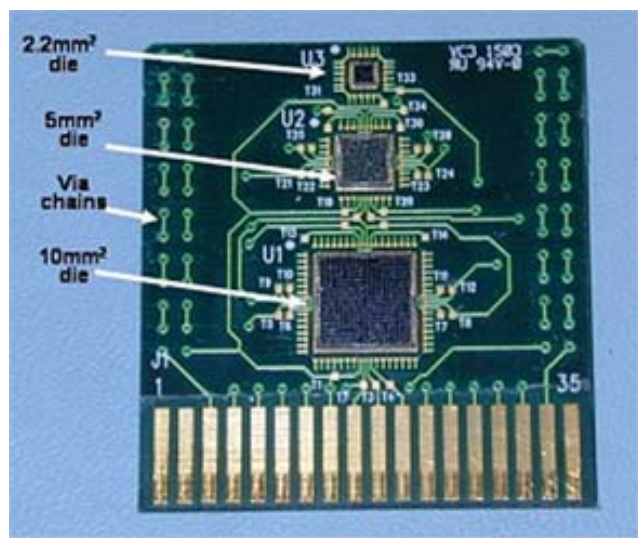matrix. Figure 3 illustrates a populated TV1 assembly on polyimide.

Figure 3: TV1- populated polyimide substrate with electronic components

The first step of the TV2 assembly process involved soldering the nano-connector to the substrate. The nano-connector leads and Au pads were pre-tinned with either In80Pb15Ag5 or Sn63Pb37 solder. Indalloy Tacflux 012 RMA (Rosin Mildly Activated) flux from Indium Corporation was used with the In80Pb15Ag5 solder. The connectors were installed and the leads were soldered onto the substrate. The hand soldering step was accomplished using a hot soldering iron at approximately 260°C for a few seconds on the In80Pb15Ag5 solder (liquidus at 154°C) and at approximately 315°C for a few seconds on Sn63Pb37 solder (liquidus at 183°C) using a custom soldering tip. After soldering, the polyimide substrates were locally cleaned with ethyl alcohol and brushed carefully in order to remove the flux. The polyimide substrates were also cleaned in the vapor degreaser for 2 minutes without immersing them into the solvent. Thick-film alumina and LTCC substrates were cleaned in the degreaser using solvent vertrel XP. Both ceramic substrates were held vertically, so the solvent drained towards the edge of the substrate.

The components, MOSFET die and resistors, were assembled and reflowed depending on the application of solder, adhesive, or a combination of both. Initially, the die area was masked by installing blue tape with a window cut out over the Au pads. The open area around the die pad was approximately 127-254 μm smaller than the die pad itself. All die attach materials approximately had a target thickness of 50.8μm. Ablebond 967-1 adhesive was screen printed onto the MOSFET die pad and dispensed onto R1, R2, and R4 resistor pads. The MOSFET and resistors were attached to the pads and the assembly was cured at 100°C +/-5°C for 4 hours. Alternatively, the In80Pb15Ag5 solder

paste (included flux) was screen printed onto the MOSFET die pad after each was pre-tinned with In80Pb15Ag5 solder wire. In80Pb15Ag5 solder paste was used to solder the resistors onto the corresponding R1, R2, and R4 pads. The solder was reflowed using two different methods: reflowed on a hot plate at approximately 170°C for 30 seconds or reflowed using infrared heat transfer at 160-170°C for 3 minutes and 40 seconds. Finally, the Zymet 6000.2 adhesive was screen printed onto the MOSFET die pad and cured at 100°C +/-5°C for 4 hours. The R1, R2, and R4 pads were soldered using In80Pb15Ag5 solder wire with Indalloy Tacflux 012 RMA flux and a hot soldering iron at approximately 180°C for a few seconds. R3 was installed upside down and bonded to the substrate with Zymet TC-611. In80Pb15Ag5 wire with Indalloy Tacflux 012 RMA flux or Sn63Pb37 wire were used to solder the 32 awg wire (Ag plated Cu buswire) from each pad on R3 to the substrate pads. This adhesive was cured along with the entire assembly.

Local cleaning was performed to remove the flux around the components that were soldered with In80Pb15Ag5 wire. The first engineering visual inspection was performed on all the test vehicles. The workmanship of the previous steps was visually inspected according to MIL-STD-883 Method 2017.7.

The polyimide, thick-film alumina and LTCC substrates were cleaned in the degreaser using Solvent Vertrel XP prior to wire bonding. An Orthodyne heavy Al wire bonder (Model 20) was used to ultrasonically bond heavy Al wire. The 127μm diameter heavy Al wire bonds were ultrasonically bonded from the MOSFET gate pad to the corresponding Au pad on the substrate. Additional 127μm heavy Al jumper wire bonds were bonded from Au pads on the substrate. The 508μm and 127μm heavy Al wire bonds were ultrasonically bonded from the MOSFET source pads to the corresponding Au pads on the substrate using a long bond tool. Destructive Pull tests were completed for each heavy Al diameter using the Microtester MCT22. All bonds passed the minimum pull strength of 300 grams for the 508μm diameter wire and 25 grams for the 127μm diameter wire per MIL –STD-883. A second engineering inspection

was performed.

Final assembly steps involved staking the nano-connector, applying the conformal coating, and taking continuity or functionality measurements. Each side of the nano-connector aluminum shell was staked or attached to the substrate with either Zymet TC-611 and cured at 100°C for 1 hour and 40 minutes or 2216 B/A and cured at 60°C for 3 hours. Dow Q1-4939 1:10 coating was applied over the entire substrate and cured at 80°C for 4 hours[4]. Parylene C coating at a thickness of 25.4 +/-12.0μm was vapor deposited onto the substrates with masked test pads[5]. The adhesion promoter or silane primer was not included because ionic shorts and failures occurred on TV1 test vehicles.

Continuity measurements of each component, performed before and after conformal coating deposition, were documented, and reworked. QA inspection occurred at 0 cycles, 500 cycles, 800 cycles, 1000, and 1500 cycles. A fully populated TV2 assembly on polyimide is shown in Figure 4.
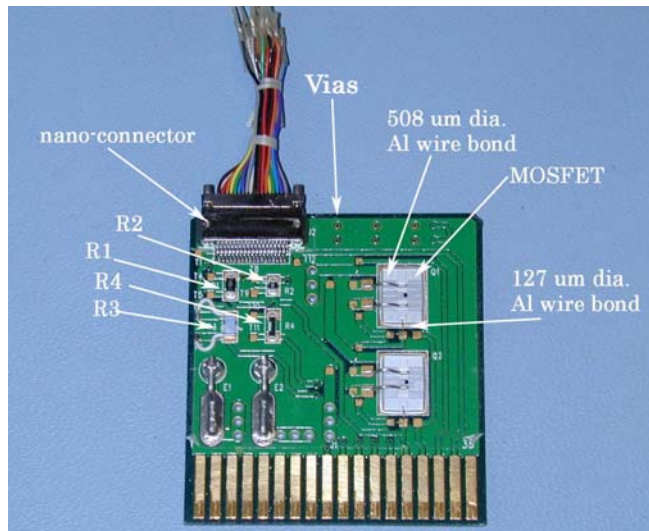
Figure 4: TV2- populated polyimide substrate with

5.4. Design of Experiments

The TV1 experiment consisted of 27 different types of test vehicle assemblies which was the result of a full factorial designed experiment. There were 10 samples of each type assembled for statistical confidence to yield a total of 270 test vehicles. Table 3 shows the TV1 full factorial matrix.

Table 3: TV1 Full Factorial Matrix

Substrate	Die attach	Encapsulant	Material	No. of Parts
Substrate 1: Polyimide				
	Die attach 1: Ablebond 967-1	Encapsulant 1	4402	10
		Encapsulant 2	Parylene	10
		Encapsulant 3	Dow Q1-4939	10
	Die attach 2: Zymet – TC-611	Encapsulant 1	4402	10
		Encapsulant 2	Parylene	10
		Encapsulant 3	Dow Q1-4939	10
	Die attach 3: Pure Indium	Encapsulant 1	4402	10
		Encapsulant 2	Parylene	10
		Encapsulant 3	Dow Q1-4939	10
Substrate 2: Al2O3				
	Die attach 1: Ablebond 967-1	Encapsulant 1	4402	10
		Encapsulant 2	Parylene	10
		Encapsulant 3	Dow Q1-4939	10
	Die attach 2: Zymet – TC-611	Encapsulant 1	4402	10
		Encapsulant 2	Parylene	10
		Encapsulant 3	Dow Q1-4939	10
	Die attach 3: Pure Indium	Encapsulant 1	4402	10
		Encapsulant 2	Parylene	10
		Encapsulant 3	Dow Q1-4939	10
Substrate 3: LTCC				
	Die attach 1: Ablebond 967-1	Encapsulant 1	4402	10
		Encapsulant 2	Parylene	10
		Encapsulant 3	Dow Q1-4939	10
	Die attach 2: Zymet – TC-611	Encapsulant 1	4402	10
		Encapsulant 2	Parylene	10
		Encapsulant 3	Dow Q1-4939	10
	Die attach 3: Pure Indium	Encapsulant 1	4402	10
		Encapsulant 2	Parylene	10
		Encapsulant 3	Dow Q1-4939	10
				270

A full factorial experiment was implemented to ensure statistical confidence on TV2. This design consisted of 180 test vehicles, including 18 different types of material combinations and 10 test vehicles of each set. TV2 Material Combination Matrix, shown in Table 4, details the component and material combinations.

Table 4: TV2 Material Combination Matrix

Substrate	No. of TVs	Serial No.	Die Attach	Heavy Al WB Dia. (mils)	Resistor (R1,2,4) Attach	R1 Endcap Finish	R2 Endcap Finish	R4 Endcap Finish	Resistor (R3) Attach	Connector Attach (Leads with SnPb finish)	Staking Material	Conformal Coating
TV2 Polyimide	10	P1-P10	Ablebond 967-1	20	Ablebond 967-1	SnPb	SnPb	SnPbAg	Zymet TC-611/Sn63	In80/Pb15/Ag5	2216 B/A	Dow Q1-4939
	10	P11-20	Ablebond 967-1	20	Ablebond 967-1	SnPb	SnPb	SnPbAg	Zymet TC-611/Sn63	In80/Pb15/Ag5	2216 B/A	Parylene C
	10	P21-30	In80/Pb15/Ag5	20	In80/Pb15/Ag5	SnPb (P30) Au (P21-29)	SnPb	SnPbAg	Zymet TC-611/Sn63	Sn 63	Zymet TC 611	Dow Q1-4939
	10	P31-P40	In80/Pb15/Ag5	20	In80/Pb15/Ag5	SnPb	SnPb	Au	Zymet TC-611/Sn63	Sn 63	Zymet TC 611	Parylene C
	10	P41-50	Zymet 6000.2	5	In80/Pb15/Ag5	Au	SnPb	SnPbAg	Zymet TC-611/Sn63	In80/Pb15/Ag5	N/A	Dow Q1-4939
	10	P51-60	Zymet 6000.2	5	In80/Pb15/Ag5	Au	SnPb	SnPbAg	Zymet TC-611/Sn63	Sn 63	N/A	Parylene C
TV2 Alumina	10	Al61-70	Ablebond 967-1	20	Ablebond 967-1	SnPb	SnPb	Au	Zymet TC-611/Sn63	In80/Pb15/Ag5	2216 B/A	Dow Q1-4939
	10	Al71-80	Ablebond 967-1	20	Ablebond 967-1	SnPb	SnPb	Au	Zymet TC-611/Sn63	In80/Pb15/Ag5	2216 B/A	Parylene C
	10	Al81-90	In80/Pb15/Ag5	20	In80/Pb15/Ag5	SnPb	Au	SnPbAg	Zymet TC-611/Sn63	Sn 63	Zymet TC 611	Dow Q1-4939
	10	Al91-100	In80/Pb15/Ag5	20	In80/Pb15/Ag5	SnPb	Au	SnPbAg	Zymet TC-611/Sn63	Sn 63	Zymet TC 611	Parylene C
	10	Al101-110	Zymet 6000.2	5	In80/Pb15/Ag5	Au (101,102) SnPb (103-110)	SnPb	SnPbAg (101,102) Au (103-110)	Zymet TC-611/Sn63	In80/Pb15/Ag5	N/A	Dow Q1-4939
	10	Al111-120	Zymet 6000.2	5	In80/Pb15/Ag5	Au	SnPb	SnPbAg	Zymet TC-611/Sn63	Sn 63	N/A	Parylene C
TV2 LTCC	10	LTCC121-130	Ablebond 967-1	20	Ablebond 967-1	SnPb	SnPb	Au	Zymet TC-611/Sn63	In80/Pb15/Ag5	2216 B/A	Dow Q1-4939
	10	LTCC131-140	Ablebond 967-1	20	Ablebond 967-1	SnPb	SnPb	Au	Zymet TC-611/Sn63	In80/Pb15/Ag5	2216 B/A	Parylene C
	10	LTCC141-150	In80/Pb15/Ag5	20	In80/Pb15/Ag5	SnPb	Au	SnPbAg	Zymet TC-611/In80	Sn 63	Zymet TC 611	Dow Q1-4939
	10	LTCC151-160	In80/Pb15/Ag5	20	In80/Pb15/Ag5	SnPb	Au	SnPbAg	Zymet TC-611/In80	Sn 63	Zymet TC 611	Parylene C
	10	LTCC161-170	Zymet 6000.2	5	In80/Pb15/Ag5	SnPb	SnPb	SnPbAg	Zymet TC-611/In80	In80/Pb15/Ag5	N/A	Dow Q1-4939
	10	LTCC171-180	Zymet 6000.2	5	In80/Pb15/Ag5	SnPb	SnPb	SnPbAg	Zymet TC-611/In80	Sn 63	N/A	Parylene C

5.5. Testing Set-up and Procedure

All TV1 and TV2 test vehicles were thermal cycled in the environmental test chamber, Tenney Model T6C-LN2, as shown in Figure 5. The volume of the inside of the chamber, approximately 30" x 30" x 30," contained a rack capable of holding up to 300 test vehicles.

Each cycle, programmed between -130°C to 92°C, averaged a 5°C/minute ramp rate. Figure 6 illustrates a typical thermal cycle temperature profile of four thermo-couples. These thermo-couples were used to ensure each test vehicle was subjected to the -120°C to 85°C temperature range. The test vehicles were thermal cycled between -120°C to 85°C and held at each temperature for 10 minutes.

Figure 5: Tenney Model T6C-LN2 Environmental Chamber
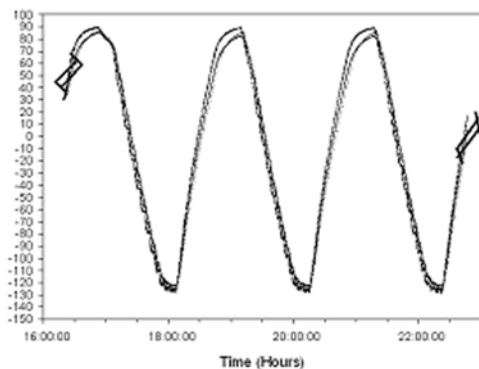
Figure 6: Thermal Cycle temperature profile of thermal couples

The test vehicles were continuously and periodically manually verified for functionality. A continuous monitoring system schematic is shown in Figure 7. The test monitoring system, located adjacent to the test chamber, had the capability of continuously monitoring 48 test vehicles simultaneously. The continuity circuits were measured for resistance three times per second and the raw resistance data was recorded on compact disk by a host computer or DAQ (Data Acquisition) system. This measuring method allowed the team to detect the beginning of an "open" failure if it was opening and closing during temperature cycling prior to remaining open with a definitive fracture. The cabling from the chamber to the monitoring system used a combination of "D" connectors and a contact fit connector. All cable solder joints exposed to temperature cycling were soldered with pure Indium solder for reliability.

For the purpose of this paper, the manual measurements are presented. These measurements were taken using an ohm meter.

All TV1 test vehicles were removed from the chamber approximately every 100 thermal cycles after an initial measurement at 0 cycles and measured for resistance. After 1500 cycles, manual continuity measurements of the test vehicles were continued to succeed 2010 cycles.

The TV2 test vehicles were measured prior to the start of cycling and taken out for their second manual measurement at 500 cycles. Measurements continued every 250-300 cycles thereafter. High resistance values or infinity indicating electrical opens were defined as failures. Quality Assurance also visually inspected the boards every 250-500 cycles after their initial inspection at 0 cycles. Following this procedure, a thorough failure analysis was executed to determine the failure mechanism or root cause, and risk mitigation.
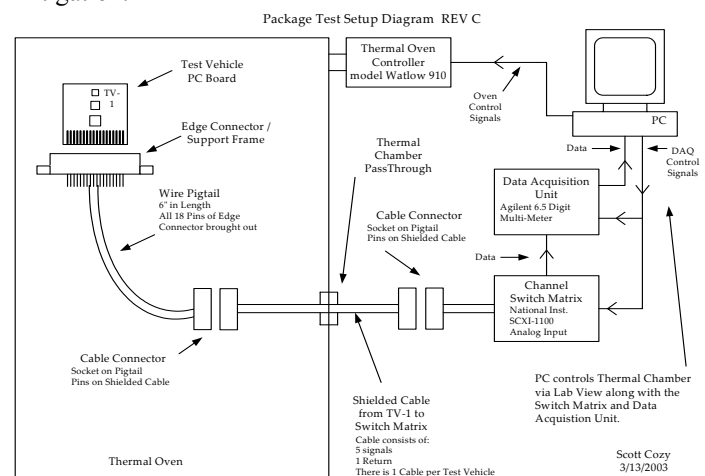
Figure 7: Continuous Monitoring System Schematic

After functionality measurements and a visual inspection were performed, the failed components were analyzed using Scanning Electron Microscopy (SEM), Fein Focus X-Ray, or an optical microscope. A selected sample was cross-sectioned, potted, and analyzed using the Hitachi S-4500 and LEO, Zeiss Supra 50 VP, scanning electron microscopes (SEM) with an IXRF Systems Energy Dispersive Spectrometer (EDS) elemental X-ray analyzer.

6. PACKAGING RESULTS AND DISCUSSION

6.1 TV1 Results and Discussion

Table 5 shows the surviving material combinations, failures, and material considerations or risk of each TV1 group. The column to the right is colored coded with red or green as a status indicator.

Inside the red or green box is the number of cycles reached when the test vehicles of that type were removed from the thermal cycling chamber. The red boxes indicate that material combination had failed and did not meet the 3X life cycle requirement. Two or more opens per lot, was the criteria for determining when the sample lot of 10 had failed (exhibited electrical open circuits); e.g. the lot defined as representing 130 circuits (10 test vehicles x 13 channels or circuits per test vehicle). In some cases where a circuit failure occurred while it was continuously monitored during thermal cycling, it was possible to determine the exact cycle in which it failed or remained continuously open. If a circuit failed that was not continuously monitored, then it would be observed during a scheduled manual resistance measurement at 100 cycle intervals. This is the reason Table 5 contains cycle counts rounded to the nearest hundred cycles on certain test vehicle types.

The range of cycles in two red boxes represents the failure that occurred within that range. The green box represents the test vehicles that are cycling to failure until each group reaches 2 or more failures. Two sets of surviving material combinations represent the current cycle counts or range of the test vehicles. The surviving material combinations also include the vias, which have not failed to date.

			CYCLES	
POLYIMIDE			10231332	
	ABLEBOND	FP4402	-1	150
		DOW	-2	250
		PARYLENE	-3	2865
	ZYMET	FP4402	-4	150
		DOW	-5	1000
		PARYLENE	-6	3247
	INDIUM	FP4402	-7	150
		DOW	-8	1000
		PARYLENE	-9	2295-2665
Al2O3			10231333	
	ABLEBOND	FP4402	-1	1400
		DOW	-2	1894
		PARYLENE	-3	1502
	ZYMET	FP4402	-4	150
		DOW	-5	800
		PARYLENE	-6	1894
	INDIUM	FP4402	-7	545
		DOW	-8	1000
LTCC			10231334	
	ABLEBOND	FP4402	-1	1894-3247
		DOW	-2	1894
		PARYLENE	-3	1600-2295
	ZYMET	FP4402	-4	150
		DOW	-5	1000
		PARYLENE	-6	1894-3247
	INDIUM	FP4402	-7	300
		DOW	-8	680
		PARYLENE	-9	2865

Table 5: Surviving TV1 Material Combinations

The failure modes identified during subsequent nondestructive and destructive failure analysis were related

to the wire bond itself in all cases. There were 5 different types of failure modes or breaks identified within the wire bond die to substrate interface as shown in Figure 8. The initial wire bond failures or circuit opens were identified at the peak or near the middle of the wire bond curve. These were observed using non-destructive X-Ray. Wire bond failures were observed several wire diameters away from the ball bond and the wedge bond, again with non-destructive X-Ray. During decapsulation of selected test vehicles, where X-Ray did not reveal any reason for a failure or open circuit, additional failure modes were observed at the ball to die and wedge to substrate interfaces.
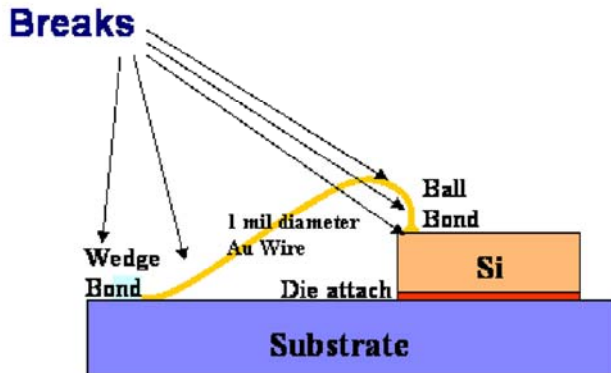
Figure 8: TV1 Five Failure Modes

For example, the illustration in Figure 9 shows the location of the open or break at or near the wire bond peak in a cross sectional view. An X-Ray image of the actual open in a test vehicle that was encapsulated with Hysol epoxy FP-4402 is shown in Figure 10.
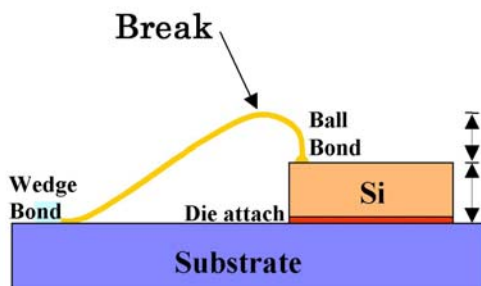
Figure 9: Location of break near the wire bond peak
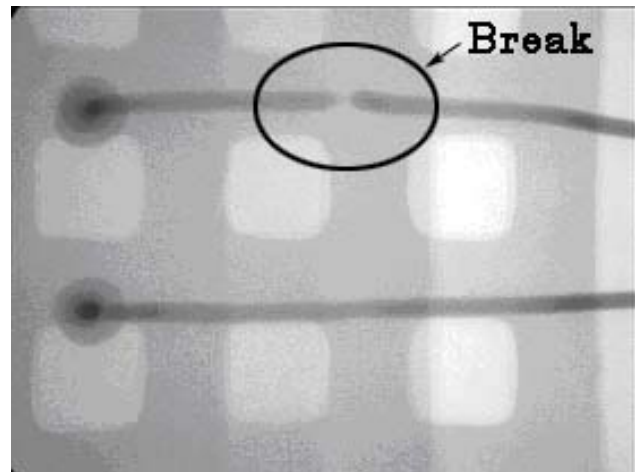
Figure 10: Fein Focus X-Ray of break near the wire bond peak

The illustration in Figure 11 & 12 shows the location of the open or break at the wedge bond to the substrate pad interface in a cross sectional view and in the high magnification picture of the actual open in a test vehicle that was decapsulated. For example, the SN: 10231332-9 lot shown in Table 5 failed after an electrical open occurred due to the Au wedge bond lifting from the Au pad (shown in Figure 12) on the substrate. The failure mode of the SN: 10231334-3 lot that failed after 2295 cycles is still under investigation.
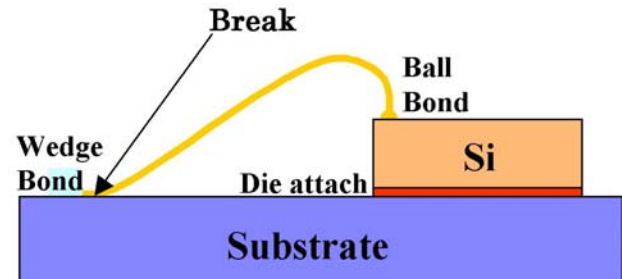
Figure 11: Location of the break at the wedge bond on the substrate
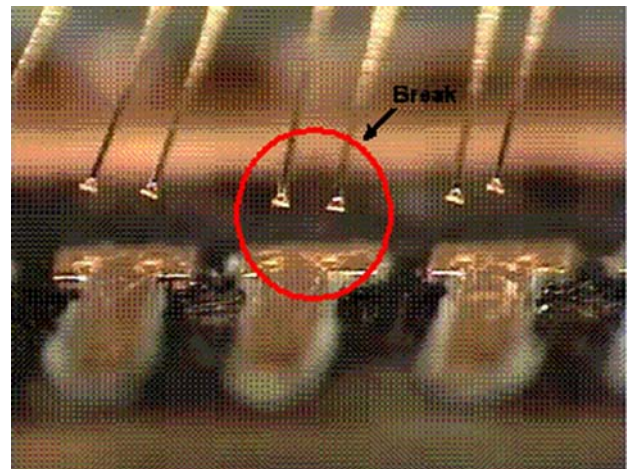
Figure 12: High Magnification of break at the wedge bond

12

During visual inspection under high power magnification X-Ray, and micro sectioning analysis, there was no evidence that a die or substrate or its metallization fractured. There was also no evidence of a via fracture. There was some evidence of encapsulant fracture, but in all cases there were multiple wire bond opens when this occurred. It should be noted that only 36 out of 270 test vehicles were destructively analyzed.

It should be noted that all test samples coated with Parylene-C did survive more than 1500 thermal cycles. The coating of Parylene-C on the Test Vehicles was approximately 25.4 μm thick. In effect the stresses induced to the Chip-On-Board assembly are minimal and if modeled are essentially negligible. In the case of the Dow material (Q1-4939) encapsulant, there are 2 types of Test Vehicles that survived more than 1500 thermal cycles. Test Vehicles encapsulated with Hysol FP-4402 resulted in 8 out of 9 combinations failing prior to reaching 1500 thermal cycles.

In wire bonds that did not necessarily exhibit opens, the effects of stress were evident in that a large strain deformation was visible. This was primarily located in the test vehicles that were encapsulated with Q1-4939. The wire bonds that failed at the die pad or substrate pad interface are likely the result of poor adhesion as a result of assembly process parameters exacerbated by oxidation or contamination. There was difficulty during the assembly of some of the first test vehicles due to contamination on the test die. Subsequently, all die were required to be plasma cleaned prior to wire bonding to ensure a good bond.

Finally, material and assembly process considerations are being investigated on TV1. From the above material considerations, In 100% will be recommended along with Parylene C coating. However, there are considerations and risk mitigation for the materials tested which will be explained further in Section 6.6.

6.2 TV2 Results and Discussion

The following Tables 6-8 present the surviving material combinations, electrical failures, and material and assembly process considerations on each substrate. Failures due to assembly and handling were eliminated from this analysis unless noted due to risk. The cycling count of each group of test vehicles is defined in a range noted in the far right column. The test vehicle with the lowest and highest number of cycles within that group of ten defines the cycling range.

The surviving components are shown in green-shaded areas on Tables 4-6. Several components that have survived the thermal cycling range and material or process/assembly considerations are defined in the far right with statistical confidence. These are also recommended for survivability in this extreme environment:

1. R1 resistor with Ni/Au endcap finish and In80Pb15Ag5 solder
2. R2 resistor with Ni/Au endcap finish and In80Pb15Ag5 solder
3. R4 resistor with Ni/Au endcap finish and In80Pb15Ag5 solder
4. 127 μm heavy Al wire wedge bonds from the MOSFET gate pad to Au pad on the substrate
5. 508 μm heavy Al wire wedge bond on the Au pad
6. Through-hole and buried vias on polyimide
7. 2216 B/A staking material
8. In80Pb15Ag5 die attach
9. Parylene C coating

SEM results showed no sign of cracks in the via metallization after 1500 cycles.

SEM analysis on the 508μm heavy Al wire bonds on one test vehicle showed that the ultrasonic wire bond on the substrate side did not penetrate through the 1.016-1.524μm thick Au plating to the Ni layer. This case has survived under these extreme temperature cycles.

The MOSFET die itself did not delaminate from the substrate. There is no evidence of die cracking. In80Pb15Ag5 solder is the preferred material to bond the MOSFET die since these power devices carry a high current. The In80Pb15Ag5 solder, which provides a rigid bonding surface, is advantageous for heavy Al wire bonding.

All red areas represent electrical failures that are defined within a cycle range of when the failure occurred or potential failures under investigation. The time of failure is defined as a cycle range of when the failure occurred between manual measurements. This cycle range is defined within the cell of the component that failed underneath the material or component type. For example, Table 6 shows 20.0 mil heavy Al wire bond failures underneath the MOSFET Die column. The first failure occurred between 638-863 cycles within the group P001-P010.

Three electrical failures have been identified: MOSFET 20 mil heavy Al wire bond lifting, nano-connector lead lifting with Sn60Pb40 finish, and R4 resistor with Sn62Pb36Ag2 endcap finish cracking through the In80Pb15Ag5 solder. The failure at R1 and R2 with Sn90Pb10 endcap finish and Ablebond 967-1 is under investigation.

The groups of each particular component electrically failed based on the following criteria:

1. MOSFET Wire Bonds: greater than1 wire bond lifted and failed out of 40 wire bonds & greater than 1 MOSFET failed out of 20 MOSFETS within each group of ten test vehicles.

2. Nano-connector Lead with Sn60Pb20 finish: greater than 1 lead lifted and failed out of 370 leads & greater than 1 connector failed out of 10 connectors within each group of ten test vehicles.

3. R4 Resistor with SnPb Endcap Finish: greater than 1 endcap cracked out of 20 endcaps & greater than 1 resistor out of 10 resistors failed within each group of ten test vehicles.

4. R1 and R2 with SnPb Endcap Finish and Ablebond 967-1[Under Investigation]: greater than 1 resistor out of 10 resistors within each group of ten test vehicles.

All 508μm in diameter heavy Al wire bonds have failed die side on each substrate according to the criteria stated above. The continuity of the 127μm in diameter heavy Al wire bonds was not considered in this study and defined in blue as a material consideration because of the unreliability of the 127μm heavy Al wedge bond on a MOSFET source pad attached with Zymet 6000.2 adhesive. This soft adhesive provided a non-rigid surface which did not quantify a reliable bond.

The connector leads have failed on a few groups of test vehicles. The time of failure is defined in the red shaded areas as a cycle range between manual measurements. All the connector attach materials that did not fail are still defined in blue as a material consideration because cracks were found at the lead toe, heel, and pad interface. Since manual measurements were taken at room temperature, the connector lead contacts could have been closed, but open at low temperature. The continuous monitoring data will be investigated in order to determine electrical failures at cold. This can also be true for the R4 resistor with SnPbAg endcap finish attached with In80Pb15Ag5 solder that did not show electrical opens at room temperature. The three main failures that have been determined (with the exception of the R1 and R2 resistors since they are still under investigation) are further described in Sections 6.3, 6.4, and 6.5. These sections also describe the risk mitigation for each failure.

The R3 Vishay (dead bug) resistor which was staked with Zymet TC-611 and attached with 32 awg wire and solder has survived, but is still under investigation and defined in blue as a material consideration since it had Sn in the SnPbAg finish and Sn63 solder was used on Ag plated Cu bus wire on polyimide substrates. The R1 and R2 resistors with Sn90Pb10 endcap finish that did not fail in other cases are also under investigation and defined in blue as well. The R1 and R2 resistors that did fail and are under investigation may have failed due to a failure mechanism involving Sn at low temperatures since obvious cracks were not found on the endcaps. This failure mechanism is further described in Section 6.4.

Several materials shown below and shaded in blue are under consideration for process/assembly and survivability purposes. The reflow of In80Pb15Ag5 solder and the 2216 B/A staking material will also be addressed as additional assembly process and function considerations. These considerations have also been mitigated as described in Section 6.6

1. Both Zymet TC-611 and 2216 B/A Nano-connector Staking Materials

2. All three MOSFET Die and resistor attach materials, Ablebond 967-1, Zymet 6000.2, and In80Pb15Ag5 solder

3. Both Parylene C and Dow Q1 4939 1:10 Conformal coatings

4. Alloys containing Sn

Table 6: Surviving Material Combinations on Polyimide

SUB.	SERIAL NO	VIA (Ohms)	MOSFET DIE ATTACH	MOSFET DIE Al wb Dia.	R1 (#)	R2 (#)	R3	R4 (# / *)	CONN. ATTACH (*)	CONN. STAKING	COAT.	TOTAL CYCLES
Polyimide	P001-010*	0.3	Ab 967-1	20 mil-638-863	Ab 967-1 638-863	Ab 967-1 638-863	Zymet TC/Sn63	Ab 967-1*	In80	2216 B/A	Dow	738-1531
	P011-020	0.3	Ab 967-1	20 mil-863-1182	Ab 967-1	Ab 967-1	Zymet TC/Sn63	Ab 967-1*	In80	2216 B/A	Pary C	1431-1918
	P021-030	0.3	In80	20 mil-638-863	In80	In80	Zymet TC/Sn63	In80*-638-863	Sn 63	Zy TC	Dow	1182-2778
	P031-040*	0.3	In80	20 mil-638-863	In80	In80	Zymet TC/Sn63	In80#	Sn 63	Zy TC	Pary C	638-2778
	P041-050	0.3	Zy 6000.2,	5 mil	In80	In80	Zymet TC/Sn63	In80*-0-638	In80-638-863		Dow	638-2678
	P051-060	0.3	Zy 6000.2,	5 mil	In80	In80	Zymet TC/Sn63	In80*	Sn 63		Pary C	2778

* SnPb finish
# Au finish
Failure Investigation
Failure
Material/process consideration
Survived

Table 7: Surviving Material Combinations on Thick –Film Alumina

SUB.	SERIAL NO	MOSFET DIE ATTACH	MOSFET DIE Al wb Dia.	R1 (#)	R2 (#)	R3	R4 (# / *)	CONN. ATTACH (*)	CONN. STAKING	COAT.	TOTAL CYCLES
Thick-Film Alumina	AL061-070	Ab 967-1	20 mil-1067-1316	Ab 967-1	Ab 967-1 623-1511	Zymet TC/Sn63	Ab 967-1#	In80	2216 B/A	Dow	623-1611
	AL071-080	Ab 967-1	20 mil-1316-1766	Ab 967-1	Ab 967-1	Zymet TC/Sn63	Ab 967-1#	In80-1067-1316	2216 B/A	Pary C	1316-2056
	AL081-090	In80	20 mil-748-1067	In80	In80	Zymet TC/Sn63	In80*-748-1067	Sn 63	Zy- TC	Dow	623-1866
	AL091-100	In80	20 mil-1766-1956	In80	In80	Zymet TC/Sn63	In80*	Sn 63-623-748	Zy- TC	Pary C	623-2538
	AL101-110	Zy 6000.2,	5 mil	In80	In80	Zymet TC/Sn63	In80*-623-748	In80		Dow	2726
	AL111-120	Zy 6000.2,	5 mil	In80	In80	Zymet TC/Sn63	In80*	Sn 63-1316-1511		Pary C	1511-2726

* SnPb finish
#Au finish
Failure Under Investigation
Failure
Material/process consideration
Survived

Table 8: Surviving Material Combinations on LTCC

SUB.	SERIAL NO	MOSFET DIE		RESISTORS ATTACH				CONN. ATTACH (*)	CONN. STAKING	COAT.	TOTAL CYCLES
		ATTACH	Al wb Dia.	R1 (#)	R2 (#)	R3	R4 (# / *)				
LTCC	L121 - 130	Ab 967-1	20 mil-1067-1316	Ab 967-1	Ab 967-1 523-748	Zymet TC/Sn63	Ab 967-1#	In80	2216 B/A	Dow	1316-2056
	L131 - 140	Ab 967-1	20 mil-1316-1511	Ab 967-1	Ab 967-1	Zymet TC/Sn63	Ab 967-1#	In80	2216 B/A	Pary C	623-2538
	L141 - 150	In80	20 mil-1067-1316	In80	In80	Zymet TC/In80	In80*-1067-1316	Sn 63	Zy-TC	Dow	1416-1866
	L151 - 160	In80	20 mil-1067-1316	In80	In80	Zymet TC/In80	In80*	Sn 63 1766 -1956	Zy-TC	Pary C	1167-2056
	L161 - 170	Zy 6000.2,	5 mil	In80	In80	Zymet TC/In80	In80*-1316-1511	In80		Dow	2726
	L171 - 180	Zy 6000.2,	5 mil	In80	In80	Zymet TC/In80	In80*	Sn 63 1511-1766		Pary C	623-2726

*SnPb finish
Au finish

Failure Under Investigation
Failure
Material/process consideration
Survived

6.3 MOSFET 508μm *Heavy Al Wire Bond Lifting—*All material combinations of 508μm in diameter heavy Al wire bonds have failed on each substrate. Failures began on polyimide between 638-863 cycles, and on thick-film alumina and LTCC between 623-1316 cycles. Electrical opens occurred due to wedge bond lifting from the MOSFET source pad. Figure 13 details the area of interest and Figure 14 shows the lifted wire bond foot on the same area. Figures 15 and 16 show a failed Al wire wedge bond interface on top of the die source pad.

The failure mode was related to micro-cracking which lead to lifting. Fatigue cracking occurred due to thermal stress generated by the thermal coefficient of expansion mismatch between the MOSFET die composed of Si (CTE = 2.49 µm/m-°C linear at 20 C)[6] and the 100% pure Al (CTE = 24 µm/m-°C linear at 20 C)[7] wedge bond [2] and ΔT.
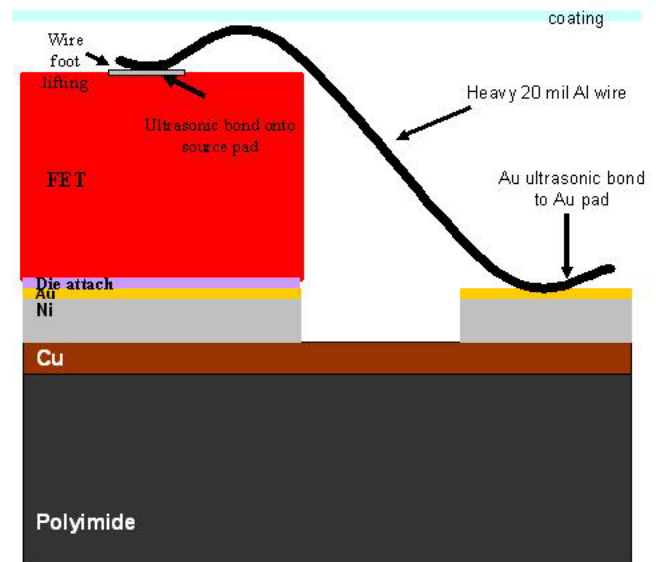
Figure 13: Schematic of Heavy Al wire bonded to MOSFET and Au Pad
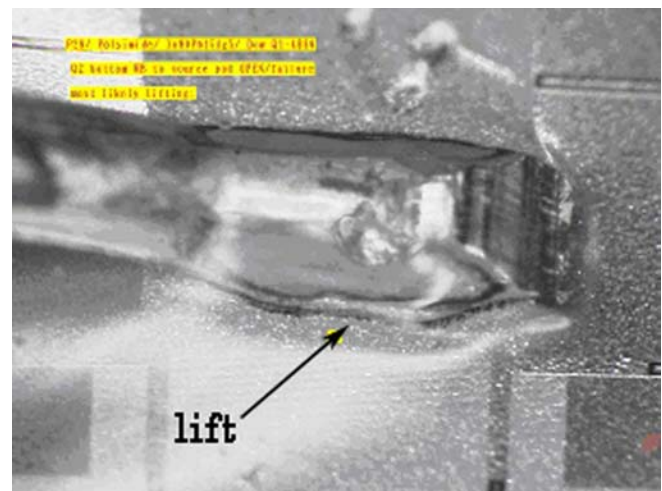
Figure 14: Top View of P029 Wire bond to Source Pad Lifting (175x)

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6 6Silicon UNS C17200, MatWeb website , http://www.matweb.com/search/SpecificMaterial.asp?bassnum=AMESi00

7 7Aluminum, UNS C17200, MatWeb website , http://www.matweb.com/search/SpecificMaterial.asp?bassnum=AMEAl00

17
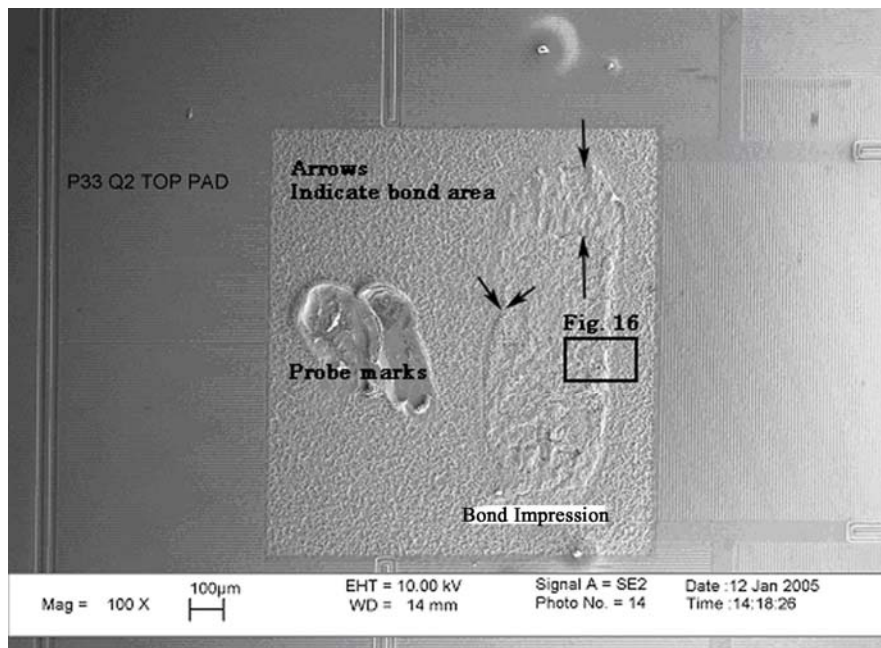
Figure 15: SEM of Failed Resgion at the source pad bond (100x and 10keV)
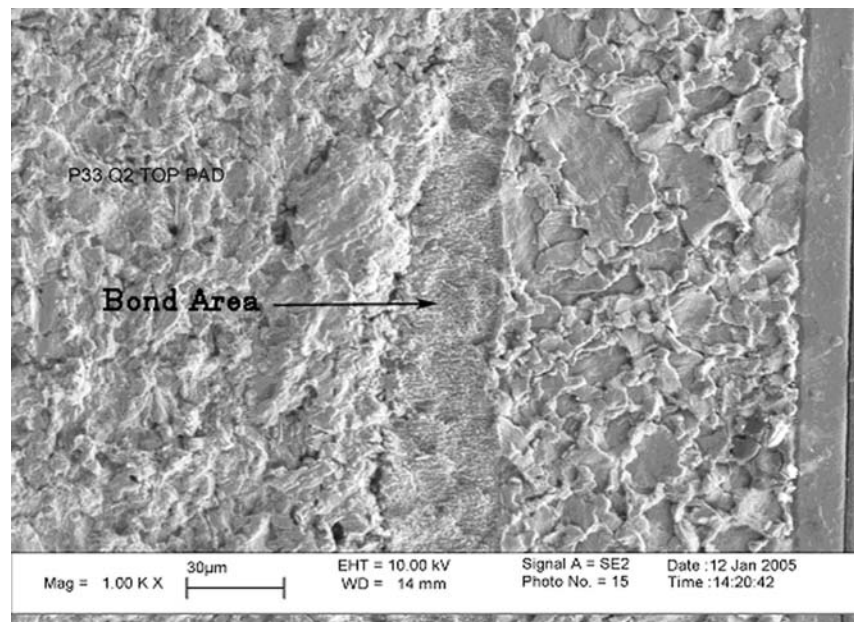
Figure 16: Detailed SEM view of failed region where wire lifted (Mag-1kx and 10keV)

International Rectifier (IR) experienced the same 508μm wire bond lifting after 6000 power cycles and 100 thermal cycles from -65°C to 150°C. IR found the failure contributed to the use of the long foot tool. After performing a Design of Experiments (DOE) on the 508μm Al wire bond process parameters and subjecting them to 150 thermal cycles from -65°C to 150°C, a short bond tool was found to significantly (95% confidence level) affect the increase in bond strength. The use of a short foot tool lead to a greater fatigue resistance [2]. However, IR recommended using 381μm diameter wire with a short tool since it had a higher reliability in reference to intermittent operating life (IOL) versus the 508μm wire with a short bond tool. More specifically, their analytical data indicated that the 381μm wire bonds survived after 15,000 power cycles versus the 508μm wire had failures after 9,000 power cycles. On Mars, the wire bonds will be subjected to both IOL and temperature cycling.

As risk mitigation, a full-factorial DOE was created to test (thermal cycle to failure) the bonding parameters of 381μm diameter heavy Al (99.99% purity) wire bonds. The test vehicles were assembled on polyimide. In80Pb15Ag5 solder preform was used to attach the MOSFETS. The assemblies were coated with Parylene C.

A standard low bonding force, standard bond loop, short bond tool, ultrasonic power and time conditions, and non-destructive pull and destructive shear tests were applied. Initially, a nominal ultrasonic power was set and used to develop an acceptable range. The ultrasonic power and time conditions were varied while the bonding force on both the die and substrate sides was kept constant at 750 grams. A die optimization test was performed using the highest ultrasonic power and time on a MOSFET die which did not reveal cracking in the Si layer.

Three ultrasonic power and three time conditions (3x3 = 9 total combinations), shown in Table 9, were varied. Two 381μm wires were bonded per die in order to accommodate the high current on TV2 polyimide substrates. A total of 16 wire bonds per bonding combination were tested in order to ensure a statistical confidence. Non-destructive pull and shear tests were performed on each bond per ultrasonic power and time setting in order to ensure a reliable bond. All wire bonds under each bonding combination passed the non-destructive pull test at 140 grams per MIL –STD-883. This showed that there was no bonding abnormalities. The results of the shear test, found in Table 9, show a typical trend, which appears to be normal for these manual bonding conditions. Manual continuity readings were taken every 100 cycles. All wire bonds under each ultrasonic power and time combination have survived after 1190 cycles compared to the 508μm heavy Al wire bonds which began failing between 638-863 cycles.

Table 9: 15.0 mil DOE- ultrasonic bonding and time combinations

S/N	Die (power (dial setting)/ time(milsec)	Substrate (power (dial setting)/ time (milsec))	Average Die Shear Force (kg-force)	Die Standard Deviation	Average Substrate Shear Force (kg-force)	Substrate Standard Deviation
1-1						
1-2	3.7/ 225	4.2/ 225	1.68	0.14993	1.57	0.15264
2-1						
2-2	3.7/ 275	4.2/ 275	1.65	0.25421	1.54	0.10234
3-1						
3-2	3.7/ 325	4.2/ 325	1.39	0.15245	1.5	0.11535
4-1						
4-2	4.2/ 225	4.725/ 225	1.45	0.40282	1.81	0.12987
5-1						
5-2	4.2/ 275	4.725/275	1.77	0.24598	1.88	0.10942
6-1						
6-2	4.2/ 325	4.725/ 325	1.75	0.185445	1.9	0.15526
7-1						
7-2	4.7/ 225	5.25/ 225	1.83	0.096126	1.88	0.19845
8-1						
8-2	4.7/ 275	5.25/ 275	2.04	0.37666	1.92	0.16939
9-1						
9-2	4.7/ 325	5.25/ 325	1.8	0.13427	2	0.28605

*6.4 Nano-Connector Lead Lifting—*Nano-connectors leads with Sn60Pb40 finish and In80Pb15Ag5 and Sn63Pb37 solder have failed on each substrate. Optical and Scanning Electron Microscopy (SEM) results have indicated that the electrical open occurred due to lead lifting. The failure mode is related to micro-cracking which lead to lifting from the Au pad.

The failure mechanism occurred due to several factors. According to literature, the failure mechanism in SnPb solder can be caused by the degradation of the mechanical properties at low temperatures and martensitic phase transformation between the phases within the solder. Sn-Pb solder is composed of α-lead cubic crystal (f.c.c.) and β-tin body-centered tetragonal (b.c.t) structures [3]. Martensite is known to form during quenching of austenitized iron-carbon alloys through a diffusionless process [4]. Rapid cooling causes atomic movement within the austenite f.c.c unit cell and transformation to a single phase of martensite with a b.c.t unit cell. Since Sn-Pb solder has the same unit cell structures, it is strongly suggested that a martensitic transform can occur from Pb with a f.c.c. unit cell to Sn with a b.c.t unit cell under cold temperature conditions. Under low temperature conditions below -110ºC, the tin phase becomes brittle [3]. Fatigue crack growth and propagation may occur in the intermetallic phase, or at the interfaces, which form the bonded joint. Fatigue cracks are also known to form underneath surface mount leads on Thin Small Outline Packages (TSOPs) under thermal shock conditions [5]. In [6], the fatigue crack growth occurred at the intermetallic compound and Sn63Pb37 bulk solder interface after thermal cycling from -35ºC to 125ºC due to shear stress from CTE mismatch between the board and chip carrier. Intermetallic compounds are typically more brittle than the bulk solder [7,8].

We believe that lead lifting can also be contributed to the poor co-planarity of the leads which ultimately affected the

soldering process. The leads had a short foot flat and showed "spring out."

The following results detail the SEM analysis on leads that lifted using In80Pb15Ag5 and Sn63Pb37 solders on polyimide and alumina substrates. Crack initiation and growth in the tin-lead finish and solder. Several mechanisms contributed to this failure: martensitic phase transformation to a Sn phase (b.c.t) unit cell at cold temperatures, brittle nature of tin, intermetallic embrittlement, and co-planarity of the leads which affected the soldering process.

Between 638 and 863 cycles, nano-connectors with In80Pb15Ag5 solder and Dow Q1 4939 1:10 silicone coating on polyimide exhibited open circuits. Between 1067 and 1316 cycles, a nano-connector lead soldered with In80Pb15Ag5 alloy failed on an alumina substrate.

Figure 17 shows a top view of a lead and subsequent cracking along the interface of the foot and the Au pad which failed between 638 and 863 cycles. The cracking along the interface caused lead lifting.
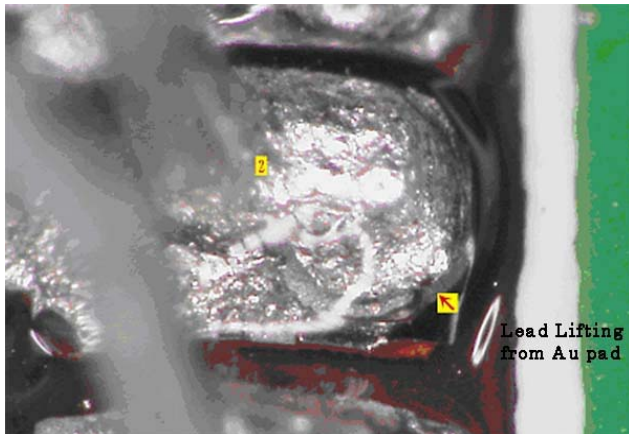
Figure 17: Top view lead lifting on PWB- P048 at 175x

The probable crack initiation site was found in the Sn60Pb40 lead finish on leads that did not fail on polyimide and alumina. Figures 18 and 19 shows the crack initiation site at the lead finish on polyimide. The failure mechanism is most likely due to a combination of martensitic phase transformation and brittle nature of Sn at low temperatures. It appears that the crack began in the lead finish and propagated into the In80Pb15Ag5 solder or possible intermetallic that formed at that interface. Figure 18 shows lead #2 that did not fail. This particular crack is underneath the lead toe, however, the failed lead in Figure 20, with a magnified backscatter image in Figure 21, showed the crack propagated through this interface at the heel or highest stress point on the package on lead #2. This corresponds to the primary crack propagation from the heel of the TSOP solder joint [5]. It is also important to note that the lead in Figure 20 most likely demonstrates poor co-planarity due to

"spring out."
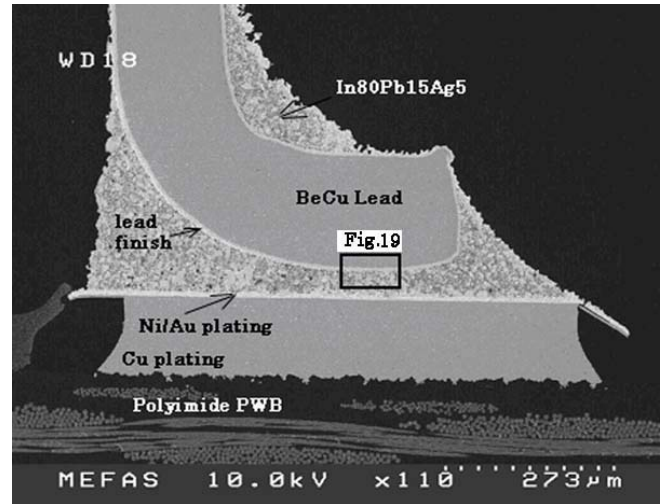
Figure 18: SEM cross- section of a lead that did not fail on polyimide at 10x and 10kev
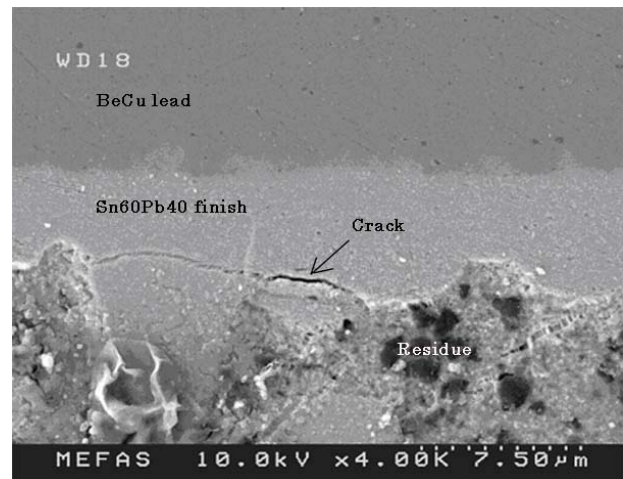
Figure 19: SEM cross- section of probable crack initiation site on polyimide at 4kx/10keV (inset from Fig. 18)

20
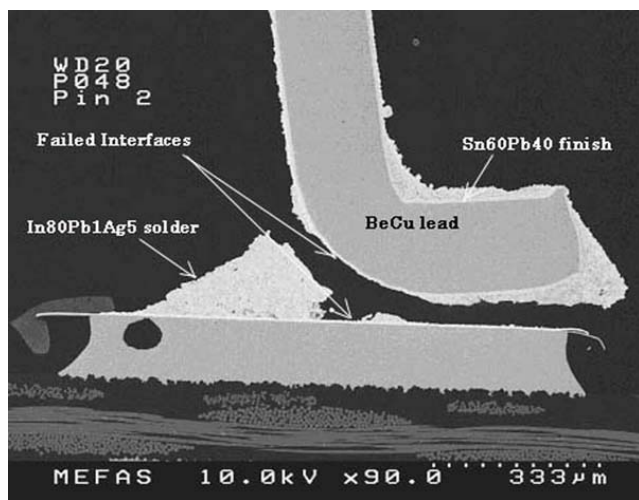
Figure 20: SEM coss- section of failed lead on polyimide at 90x/ 10keV
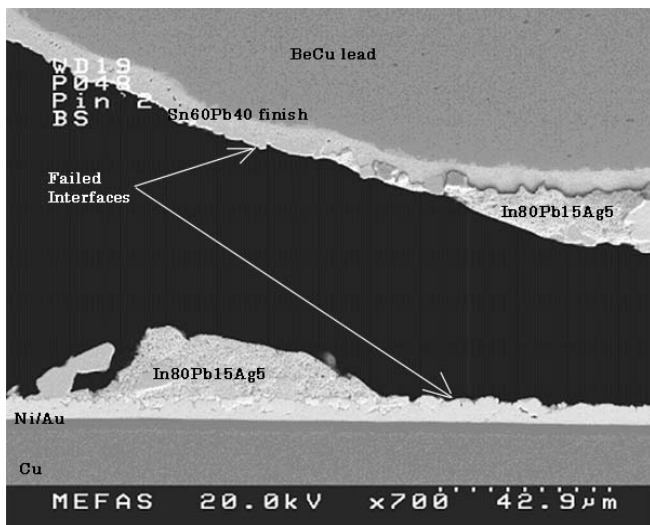
Figure 21: Back-scatter image of failed interfaces at 700x/20keV

Even though the BeCu lead and polyimide PWB have closely matched CTE of 17.0 μm/m-°C[8], and 16.50 μm/m-°C in the x, y-direction [9], respectively, the In80Pb15Ag5 solder has a CTE of 28 ppm/C.[9]
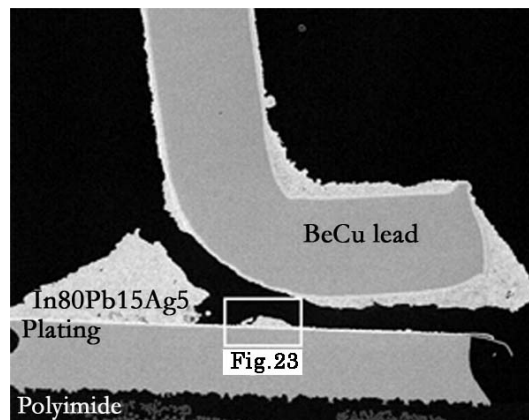
Figure 22: SEM cross- section of intermetallic analysis location at 90x/10keV

21 ⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯⎯

Local stresses and volume changes within the microstructure due to the martensitic phase transformation of the FCC lead phase to a BCT Sn phase and loss of ductility of Sn phase were most likely integral in causing the crack to initiate at the Sn60Pb40 lead finish. It is suspected that both mechanisms caused crack propagation and separation at the interface. It is undetermined if the crack began in the Sn phase, but most likely occurred due to the phase transformation at low temperatures.

A secondary crack propagated at the In80Pb15Ag5 solder and PWB interface as shown in Figures 9. This crack propagated into the second failed region in proximity to the Cu/Ni/Au (1.016-1.524 μm) plating interface. It is possible that the fatigue failure occurred at this interface due to fatigue stress. Repetitive thermal cycling caused cyclic strains in the solder joint mainly due to the magnitude of the change in temperature of 205°C and the difference in CTE between the BeCu lead, In80Pb15Ag5 solder, and the PWB.

[8]Beryllium Copper, UNS C17000, MatWeb website , http://www.matweb.com/search/SpecificMaterial.asp?bassnum=MCUABA10

[9] Master Solder Alloy Properties Table, from the Indium Corp. website < http://www.indium.com/products/oldalloychart.php> accessed November 2, 2004

Figure 23: Magnified View of Inset in Fig. 22 at 3kx/
20keV

A detailed analysis of the intermetallics is described in [10]. Several intermetallic compounds formed with Sn were found at the interface near where the crack propogated. This shows that Sn is integral in intermetallic embrittlement since it is known to lose ductility under low temperature conditions [3].

Crack initiation and propagation occurred within the eutectic Sn63Pb37 solder that was used on the connector leads. Visual inspection revealed a crack at the heel fillet, highest stress point, as shown in Figure 24 at lead #6 of the failed pair, #6 and #31 that are daisy chained. SEM analysis revealed cracks under the heel of both leads #6 and #31. Crack propagation occurred near the plating interface in the solder in both Pb (light region) and Sn (dark region) phases. However, it is more likely that the cracks began in the Sn phase due to the phase transformation and brittle nature of tin at low temperatures. Figures 25 and 26 show several cracks through the solder under the lead foot and finish of leads #6 and #31. The cracks within the trace in from the lead in Figure 26 were caused from sample preparation.

Figure 24: Top View of Crack at Heel of Lead #6 in the front with Sn63 solder on Alumina and Parylene Coating (175x)
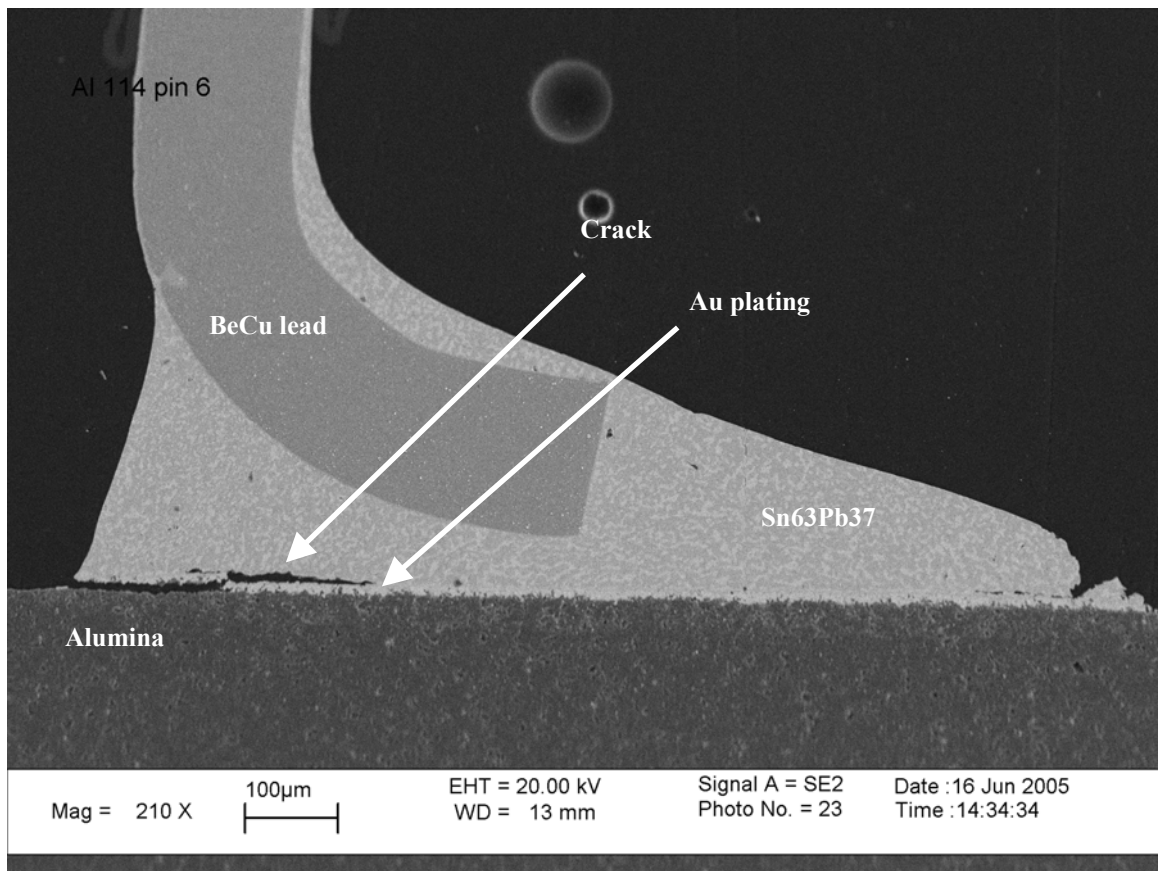
Figure 25: SEM Cross-Section of Al114 Failed Lead Foot #6 in the front at Mag- 210x and 20keV
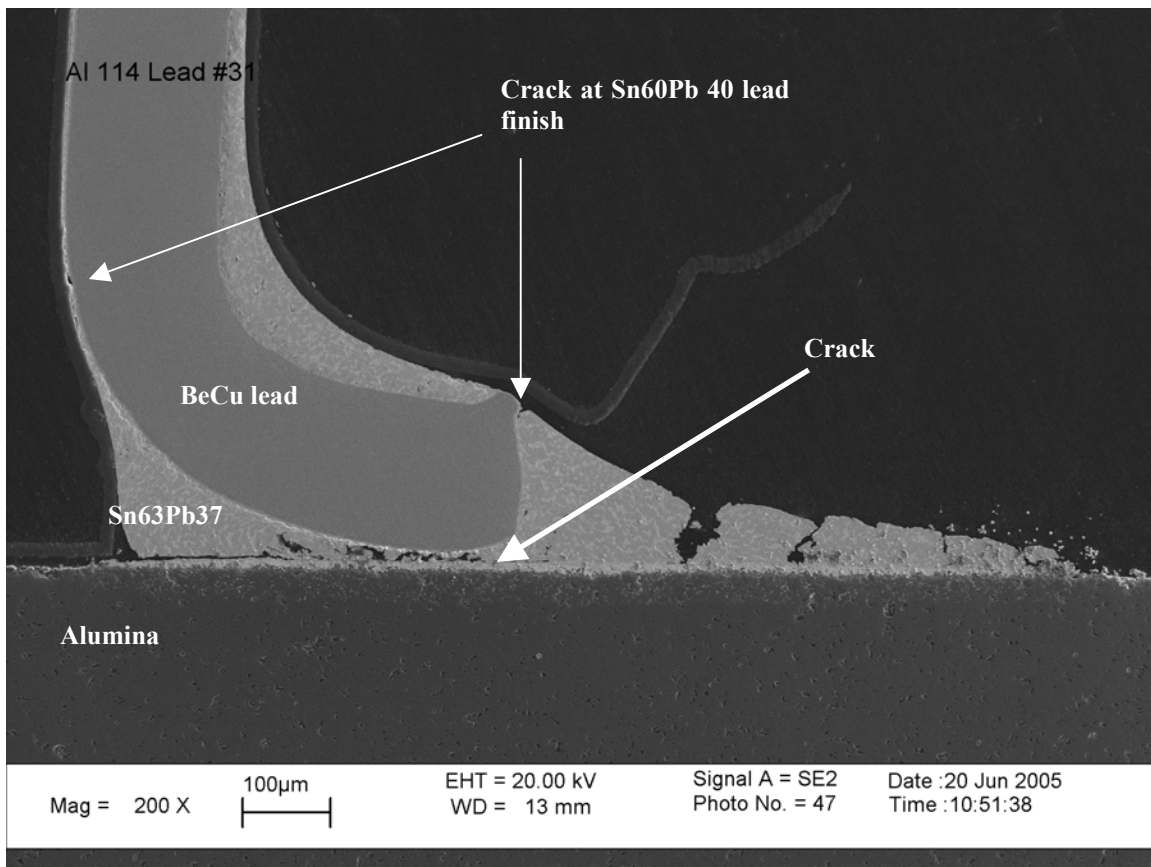
Figure 26: SEM Cross-Section of Al114 Failed Lead Foot #31 in the back at Mag- 200x and 20keV

Figure 27 shows a map of the leads that failed on each row of the 37-pin nano-connector. It must be noted that the sum reflects the number of leads that failed when the initial open circuit occurred.

Back Row	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	Lead Number	
	0	0	2	2	0	1	2	0	1	0	0	0	2	0	1	2	0	1	1	# Failed Leads:	15
Front Row	1	2	3	4	5	6	7	8		9	10	11	12	13	14	15	16	17	18	Lead Number	
	0	1	1	1	1	2	0	1		1	0	1	3	1	1	2	1	1	0	# Failed Leads:	18

Figure 27: Map of the nano-connector leads that failed on each row

There is not a significant difference between the number of leads that failed between the front (18 failed) and back rows (15 failed), so the stiffness of the shorter leads in the back row is not believed to be a factor in the failure mechanism. The distribution of leads that failed throughout each row is fairly even. It must be noted that lead #37 was not probed individually and could result in additional failures, but it is not statistically signficiant.

The results in Figure 27 suggest that this is an alloy problem and not a stress problem due to the structure being in a fixed-fixed position resulting in a maximum deflection and stress at the mid-point area. We plan to experimentally test a structural adhesive underneath the aluminum shell versus using the fasteners. If the result is similar, then we can conclude that the failure is due to the mechanisms stated

earlier in this section: intermetallic embrittlement, martensitic phase transformation, etc. However, the structural attach material would take the majority of the load and could fail due to creep or fracture under these extreme temperature and thermal cycle conditions.

As risk mitigation, nano-connectors with Au lead finish and In80/Pb15/Ag5 solder will be thermal cycled. A new tool was purchased at the vendor in order to manufacture a longer foot flat of 508μm versus 127μm for better reliability. This longer foot flat is closer to the recommendation in [11]. Both typical foot flat of 127μm and extended foot flat of 508μm will be tested. Each nano-connector will continue to be fit-checked to the board. The lead co-planarity will be inspected and the leads will be reworked in order to ensure proper placement on the pads. The extended foot is also beneficial for co-planarity reasons because bending the 127μm lead flat to the surface proved difficult. The leads and pads will continue to be pre-tinned with the In80/Pb15/Ag5 solder. The soldering process will be practiced and a custom solder tip will continue to be used. A structural attach material will also be investigated.

*6.5 R4 Resistor Endcap Cracking—*Electrically open circuits have occurred at the R4 resistor with Sn62Pb36Ag2 finish and In80Pb15Ag5 solder starting between 0-563 cycles on polyimide. The failure mode is related to cracking through the endcap solder as shown in Figure 28. The failure mechanism occurred due to the absence of a Ni layer which cannot structurally hold the solder, as shown in Figure 29. A Ni layer functions as an adhesion layer and interdiffusion barrier. This resistor had the largest package size, 1506, which induced the highest thermal stress.
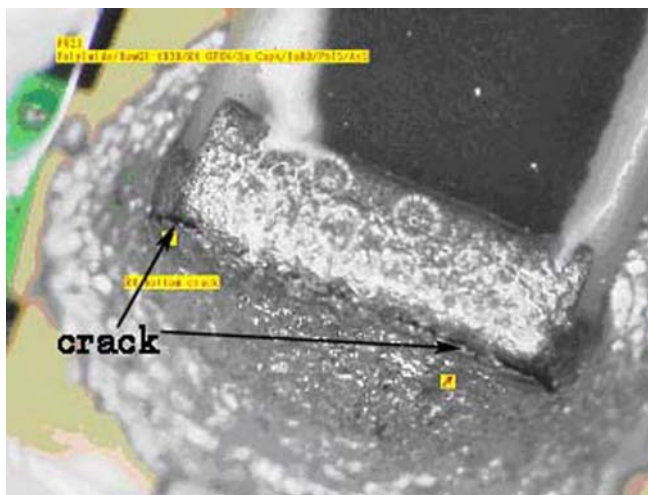
Figure 28: Top View of R4 Sn/Pb/Ag Finish Endcap Cracking using In80/Pb15/Ag5 Solder on Polyimide (175x)
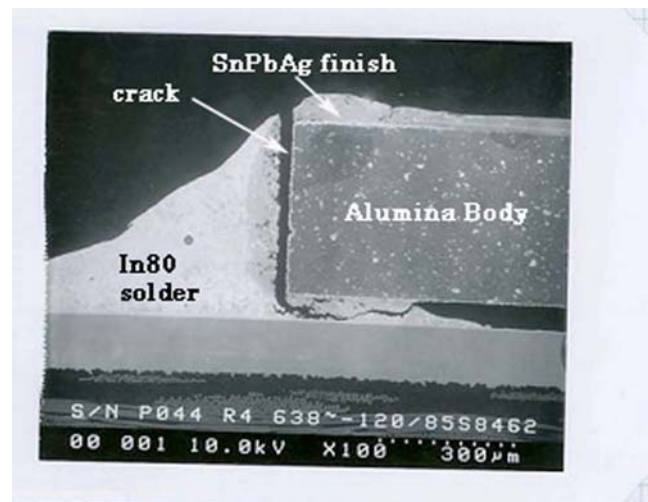
Figure 29: SEM Cross- Section View of R4 Endcap Cracking at Mag-100x and 10keV

As risk mitigation, resistors with Ni/Au endcap finish and In80Pb15Ag5 solder will continue to be used since they have survived cycling.

*6.6 Material, Assembly/Process Considerations—*Considerations of the staking, die, conformal coating, and finish or solder materials from the TV1 and TV2 experiments have been made. Risk mitigation has been applied to each area.

The staking material is important for the nano-connector tested in TV2 to withstand vibration testing (simulating launch) and mating and demating of the nano-connector plug. After 500 cycles, the Zymet TC-611 staking material used to attach the nano-connector aluminum shell failed on 30/60 test vehicles. The Zymet TC-611 is a soft, tacky material that attracts debris, and detached from the aluminum shell. Between 0-500 cycles, a single crack was found in the 2216 B/A staking material on one side of the nano-connector, however cracks were found throughout the test vehicles after continued thermal cycling. The connector that exhibited an open using 2216 B/A did not exhibit cracks. Even though 2216 B/A exhibited cracks on other connectors that did not catastrophically fail and showed an open at room temperature, we conclude that cracking did not contribute to the failure mechanism and this material is still under consideration. Additional staking materials are under investigation.

The Zymet 6000.2 die attach material on TV2 will not be pursued as a die attach material since it was reliability risk for heavy Al wire bonding on TV2. Using the In80Pb15Ag5 solder as a die attach material to bond the MOSFET in the ambient resulted in voiding from 10-80. This is also true for In 100% used on TV1. The assembly process of In has been mitigated by reflowing in a vacuum which is also a more reliable and consistent process.

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Using Ablebond 967-1 adhesive during assembly was a risk since it has a low viscosity. Ablebond 967-1 was used on TV1 and TV2. One out of 180 TV2 test vehicles had a short at 0 cycles during the assembly process because the adhesive bleed together between the resistor pads. A cross-sectional analysis using SEM also showed bleed out between the pads. Additional assembly practice concluded that the Ablebond 967-1 causes bleed-out problems. Bleed out has occurred on Au bonding pads that were in proximity to the die pad, and in-between small package sizes such as 0603 and 0402. Additional passive and die attach materials with higher viscosity are being investigated in order to prevent bleed out and potential shorts between pads and traces in proximity to the bond pads. Currently, Ablebond 84-1 is being pursued since APL's PoF experiment (similar to TV1) resulted in 0 failures after 1500 cycles on polyimide with Parylene C coating [12]. Cracks were not found after 1500 cycles [12]. The compliance and glass transition temperature of other materials will also be investigated.

The Dow Q1 4939 conformal coating is tacky and attracts debris. Outgassing is a concern and rework using this silicone material may cause contamination problems, especially on the wire bond pads. Parylene C began peeling away or lifting from the traces, components, and edges on TV2 where it was masked on each substrate between 0-500 cycles. This lifting could have occurred due to the absence of silane primer or contamination. Parylene C conformal coating also began to peel from traces on TV2-1 (15 mil Wire Bond DOE). This lifting became obvious at 412 cycles, but it also could have begun earlier. Another disadvantage of using Parylene-C is that it does not provide any mechanical protection to the wire bonds during handling or service use. Rework is a concern because removing 1 mil thickness is very difficult and re-depositing it in local areas can cause a difficult masking procedure. Parylene C coating will continue to be used and rework strategies using this coating are being explored. The substrates will continue to be cleaned with a vapor degreaser in order to decrease the contamination. The advantage of silane primer in a vaporized form is also under investigation.

Finally, the choice of a component finish or solder material with Sn is a risk to survivability under these low temperature conditions. Alloys with Sn will not be used on future experiments.

7. TCRE ELECTRONICS EXPERIMENTAL DETAILS, RESULTS AND DISCUSSIONS

A list of COTS used for the control of actuators encompasses discrete transistors, digital gates, mixed signal circuits, and analog CMOS amplifiers. A short functional/non functional test down to -180°C was first conducted to characterize the electronics at low temperatures and then a 1000-hour power-on steady-state life test was performed at -150°C. An Operational Amplifier was also designed using design-for-reliability approach to ensure long term reliability under the wide temperature range of +85C to -135C.

7.1. Cold Short Term Testing

The low temperature testing was conducted at temperatures ranging from room temperature (20ºC) to -180ºC on the following electronic devices: Diodes Fairchild IN4148, IN5819, IN5711, IN5242, 2.IN5352; Voltage Reference Diode Linear Technology LT1029; Voltage Reference Diode National LM185-1.2/2.5; Gate Driver International Rectifier RIC7113A4; Current Regulator Diode Interfet J554; MOSFET International Rectifier IRHG57110; DC-DC Converter Interpoint SMSA 2805S and MSA 2805S, Capacitor Ceramic 1uF 10V X7R C0805; Resistor 10-Ohm P2010E10RBB and 40-kOhm; VFC150640K000FBT; Oscillators VPC1-E3F-32M; Schmidt Trigger HCS14; Fuses R459.250 and R451015.

Diode

One Fairchild diode IN4148 and two of IN5819, IN5711, IN5242 and IN5352 were tested at temperature range of 5ºC ~ -184ºC. The DUTs were biased under both forward and reverse bias conditions by a Tektronix 576 Curve Tracer and the IV curves under those bias conditions were recorded at each test temperature.

The voltage when forward current is 20uA is defined as Von and the reverse breakdown voltage is denoted as Vbd. Figure 30 plots the parameter Von as a function of temperature. Figure 31 gives the relationship of Vbd and ambient temperature. Both Von and Vbd parameters are read off the IV curves recorded by the Tektronix Curve Tracer.

Shown in Figure 30, the Von of IN4148, IN5819 and IN5711 has at least 100% change over the temperature while Von of IN5242 and IN5352 have about 45~50% change at the same temperature range. The change of the reverse breakdown voltage is more consistent for all diodes, which shows an overall 15~20% decrease from 5ºC to -180ºC.
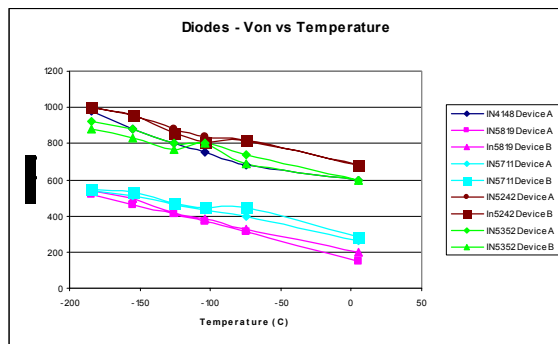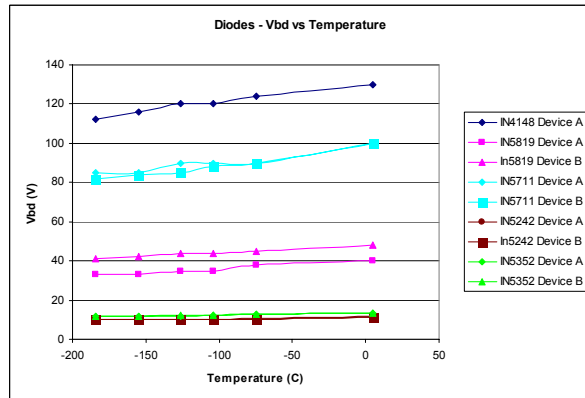
Figure 30. Von as a function of temperature.

Figure 31. Vbd as a function of temperature.

Voltage Reference Diode

Two 5V Bandgap Reference Diode LT1029, two 2.5V Micropower Voltage Reference Diode LM185-2.5 and two 1.2V Micropower Voltage Reference Diode LM185-1.2 were tested at a temperature range of 100ºC to -180ºC with no larger than -25ºC step. It took 5-10 minutes for each step and 5 minutes to reach steady-state. Each measurement was taken at the stabilized temperature. All the diodes were biased by a Keithley 4200 under reverse current condition range from 100uA to 10mA and reverse voltage was reordered during the reverse current injection. The interest of the investigation is the millivolt accuracy under three currents, 1mA, 3mA and 7mA.

All the diodes were operating fairly well at the temperature range of 100ºC to -150ºC. Under -180ºC, LT1029 was within 50mV change up to 9mA, while LM185s lost their functionality as reference diodes. 5ºC step from -180ºC to -150ºC for LM185-1.2V indicated that -150ºC was the threshold temperature for the diode performance with 1.5% to 7% shift from 1.2V. Figure 32 shows reverse voltage change from 100ºC to -180ºC under the three currents of interest for LM185-1.2V.

Figures 33, and 34 show the reverse voltage change as a function of temperature from 100ºC to -180ºC under the three currents of interest for LM185-2.5V and LT1029, respectively. It seems that -150ºC is the temperature

threshold for all three diodes. The difference is LM185s began to have over 10% change below -150ºC, while LT1029 was operating with approximately 50mV change down to -180ºC.
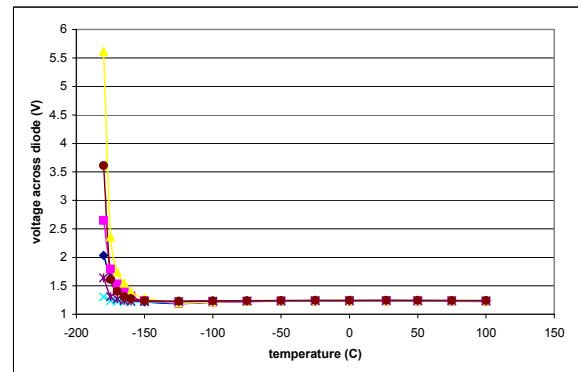
Figure 32. Voltage at different current biases as a function of temperature for LM185-1.2.
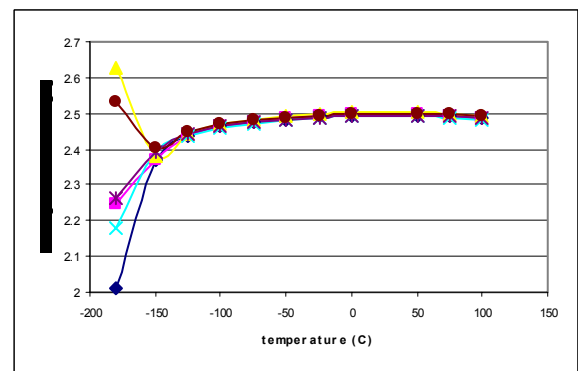
Figure 33. Voltage at different current biases as a function of temperature for LM185-2.5.
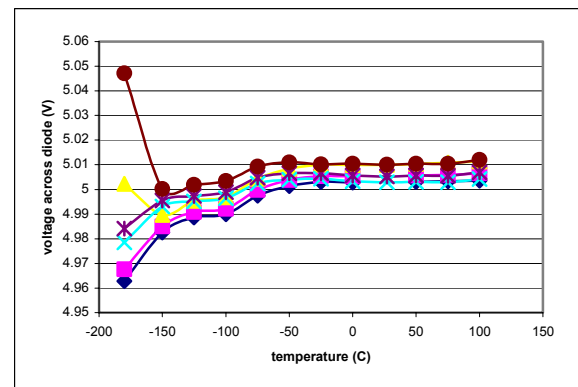
Figure 34. Voltage at different current biases as a function of temperature for LT1029.

Current Regulator Diode

A sample size of two current regulator diodes, Interfet J554, was tested at temperature range of 5ºC ~ -184ºC. The DUTs were forward biased by a Tektronix 576 Curve Tracer and

the forward IV curves were recorded at each test temperature. Both J554 have the same temperature dependent trend, but there is an obvious statistical variation of the two devices.

MOSFET

The International Rectifier IRHG57110, a quad MOSFET, was tested at temperature range of 5ºC ~ -184ºC. The DUTs were biased by a Tektronix 576 Curve Tracer and the IV curves were recorded at each test temperature. Rdson was calculated from the recorded IV curves when Vds was 12V. Threshold voltage, Vth, was the gate voltage when the DUTs were biased at Vds and Ids equal to 1V and 1uA, respectively.

Figures 35-37 plot the Vbd, Rdson and Vth as a function of temperature and show a clear trend of temperature dependence of these parameters.
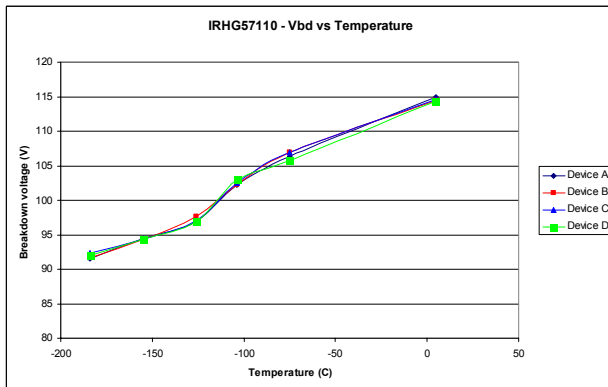
Figure 35. Vbd of IRHG57110 as a function of temperature.
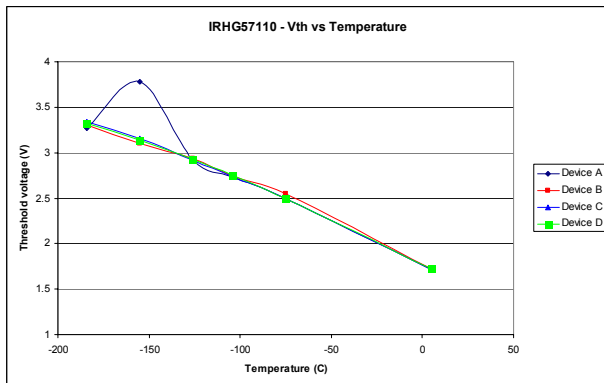
Figure 36. Vth of IRHG57110 as a function of temperature.
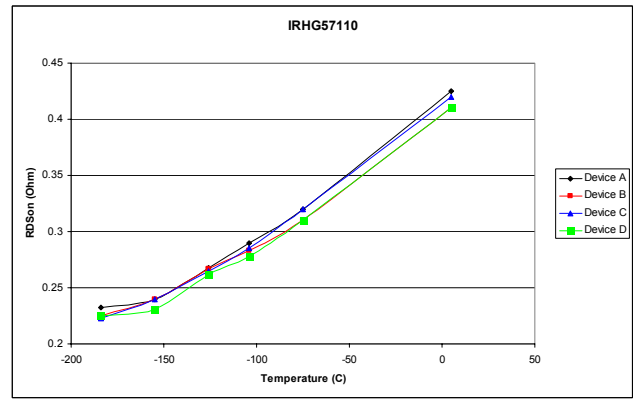
Figure 37. Rdson of IRHG57110 as a function of temperature.

In addition, one IRHLF77024 and one IRHLF797024 were tested by an HP4145B at temperatures ranging from 22ºC to -180ºC. The Rdson was calculated at Id=100 mA and Vth was measured when Vds=100 mV with Vgs sweeping from 0 to 3V in 10mV steps. The breakdown voltage, Rdson and Vth as function of temperature are given in Figures 35(a), 36(a) and 37(a).
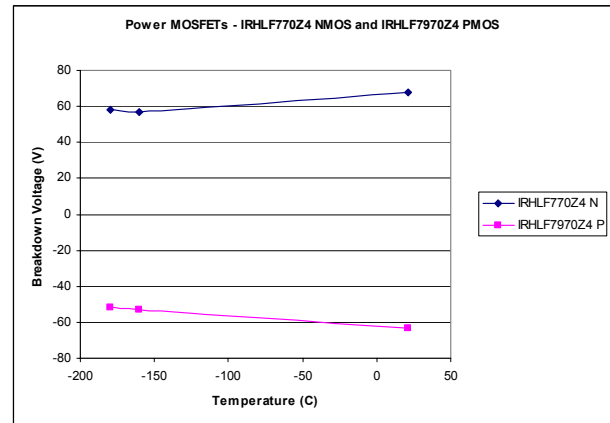
Figure 35(a). Vbd as a function of temperature.
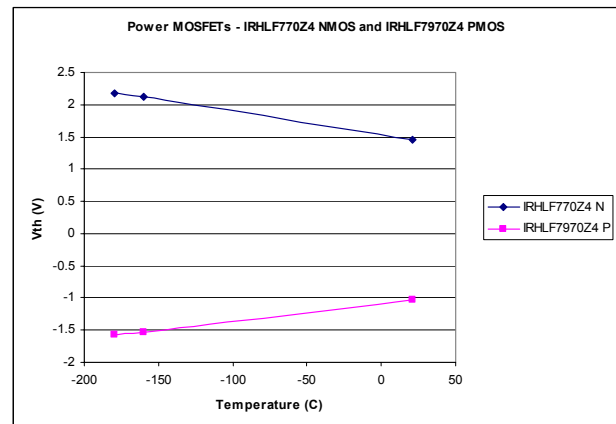
Figure 36(a). Vth as a function of temperature.
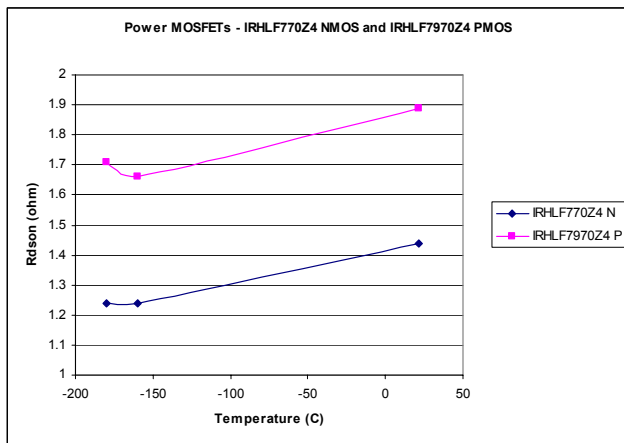
Figure 37(a). Rdson as a function of temperature.

Gate Driver

A single gate driver, International Rectifier RIC7113A4, was tested at temperature range of 5ºC ~ -184ºC. Two Agilent E3616A DC Power Supplies were used as the 15V and 5V input voltage sources for the DUTs. The output was recorded by a Tektronix TDS744a Oscilloscope and an HP8116A Pulse Generator was used to generate the input signal.

Keeping the 5V logic supply voltage unchanged, the gate drive voltage was then reduced gradually to a point when the devices stopped outputting. This gate drive is defined as the dropout voltage. Then the gate drive voltage supply was increased gradually to a point when the devices started outputting again. This gate drive is denoted as recovery voltage, shown in Figure 38 as function temperature.
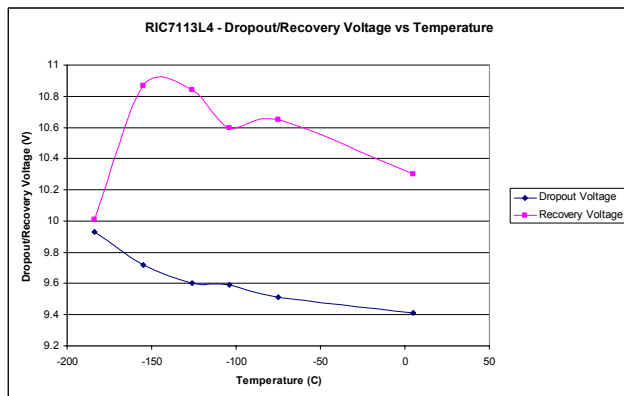
Figure 38. Dropout/Recovery voltage of RIC7113A4 as a function of temperature.

DC-DC Converter

A total of four DC-DC converters, two Interpoint SMSA 2805S and two Interpoint MSA 2805S, were tested at temperatures ranging from of 5ºC to -126ºC. The DUTs were tested at output powers of 0.25W, 3W and 5W. An

Agilent E3634A DC Power Supply was used as the 36V input voltage source for all the DUTs. The output was recorded by a Tektronix TDS744a Oscilloscope.

-150ºC destroyed one of SMSA 2805S devices and one of MSA 2805S. One device drew over 1.2A at the temperature as soon as it was switched on; the other had 388mA and the output was unregulated at 16.1V and spiked off the scale. Figures 39 through 41 show the mean output voltage, output current and input current with no load as function of temperature for the four DUTs.

Shown in Figure 39, the output voltage is relatively insensitive to temperature down to -75ºC, but starts to fluctuate without a clear trend from -75ºC to -180ºC. The output power impact is clearer with higher output voltage at higher power.

Output current and input current without load are much consistent with temperature with input current starting to go up with lower output power, shown in Figures 40 and 41.
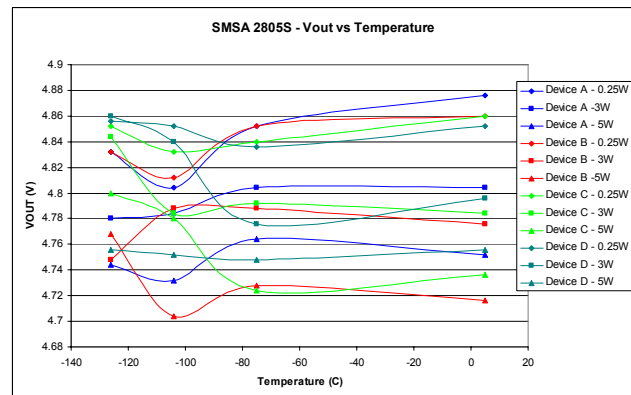

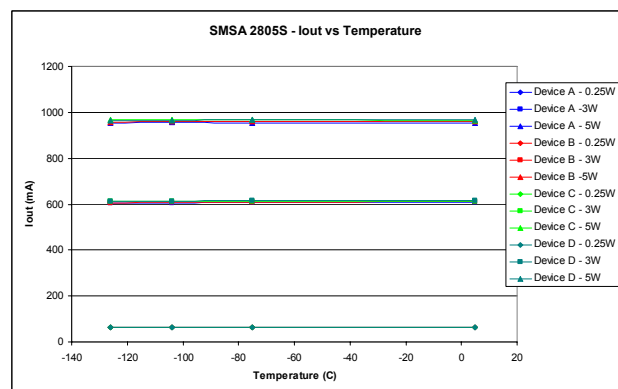Figure 39. Output voltage of SMSA 2805S as a function of temperature.

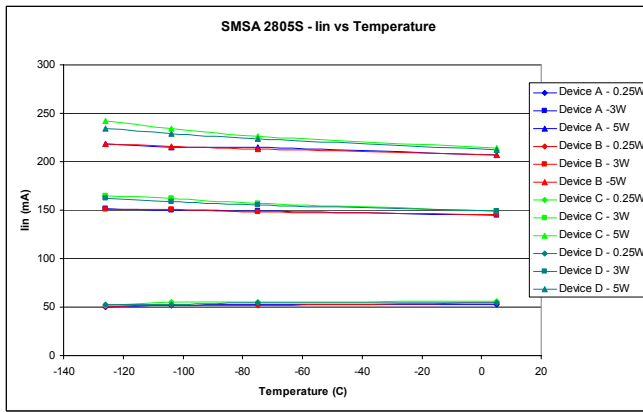Figure 40. Output current of SMSA 2805S as a function of temperature.

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Figure 41. Input current of SMSA 2805S as a function of temperature.

Capacitor

One ceramic 1uF 10V X7R C0805ZC105JAT2A from AVX was tested by a HP 4275A LCR meter from the temperature range of 22ºC to -180ºC. The percentage increase of capacitance over the temperature range is about 65% and the percentage decrease of the dissipation factor over the temperature range is 50%.

Resistor

One 10-Ohm P2010E10RBB and one 40-kOhm VFC150640K000FBT were tested by HP 34401A Multimeter from the temperature range of 22ºC to -180ºC, The change of resistor over the temperature range is 0.1~0.2%.

Oscillator

A sample size of two oscillators, both VPC1-E3F-32M, were tested using a Power Supply HP 6235A for biasing and a frequency counter, Stanford Research Space Model SR620, and DMM Fluke Model 87V over temperature range of 22ºC to -180ºC. Figures 42, 43, 44, and 45 give the dropout voltage, frequency, disabled supply input current and enabled supply input current as function of temperature, respectively. Except for the enabled supply input current which shows significant variations between the two test samples, other parameters matched well and display clear temperature dependence.
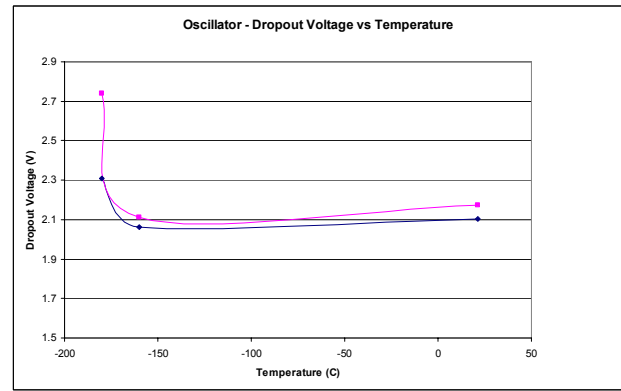
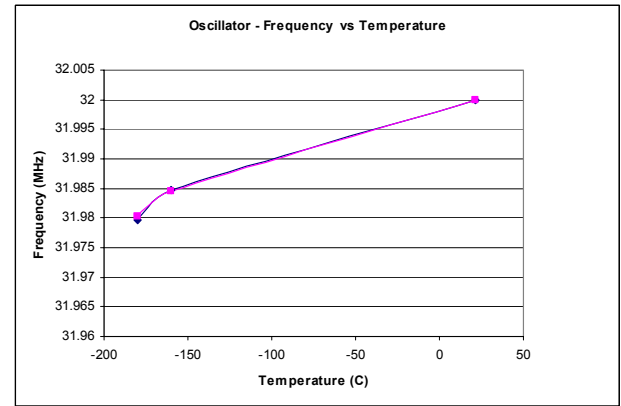Figure 42. Dropout voltage as a function of temperature.

Figure 43. Frequency as a function of temperature.

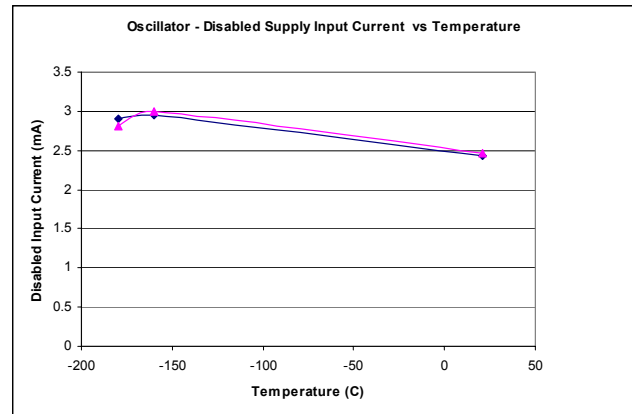There is approximately 0.06% change of the frequency over the temperature.

Figure 44. Disabled supply input current as a function of temperature.
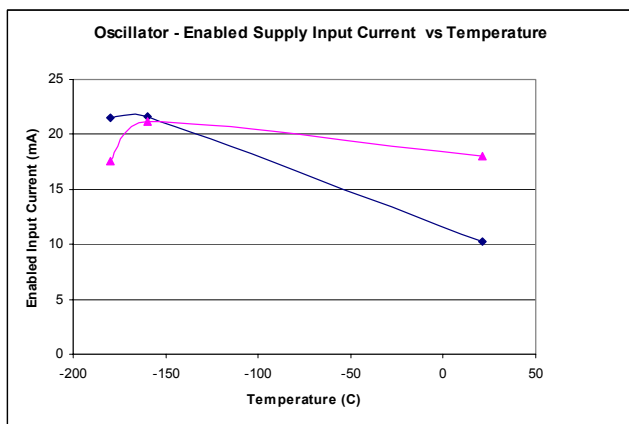
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Figure 45. Enabled supply input current as a function of temperature.

Inverter HCS05

A single inverter, HCS05, was tested at temperature range of 5ºC ~ -184ºC. An Agilent E3616A DC Power Supplies was used as the 5V input voltage source and an HP8116A Pulse Generator was used to generate the input signal. The output was recorded by a Tektronix TDS744a Oscilloscope.

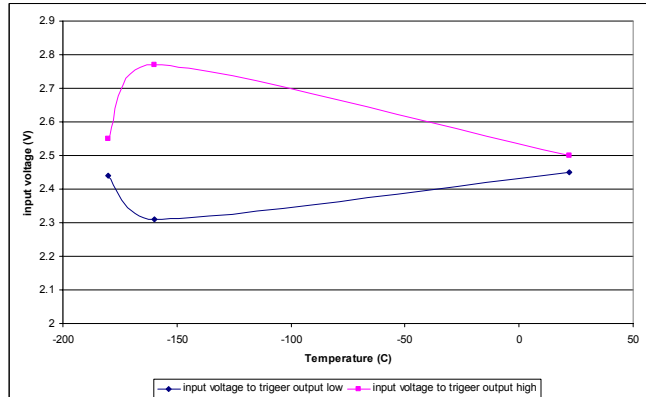Figure 46 shows the input voltage to trigger the output high and the input voltage to trigger the output as a function of temperature.

Figure 46. Input voltage to trigger output high and output low as a function of temperature.

Schmidt Trigger HCS14

A single Schmidt Trigger, HCS14, was tested at temperature range of 22ºC ~ -180ºC. An Agilent E3616A DC Power Supplies was used as the 5V input voltage source and an HP8116A Pulse Generator was used to generate the input signal. The output was recorded by a Tektronix TDS744a Oscilloscope.

Figure 47 shows the input voltage to trigger the output high and the input voltage to trigger the output low as a function of temperature.
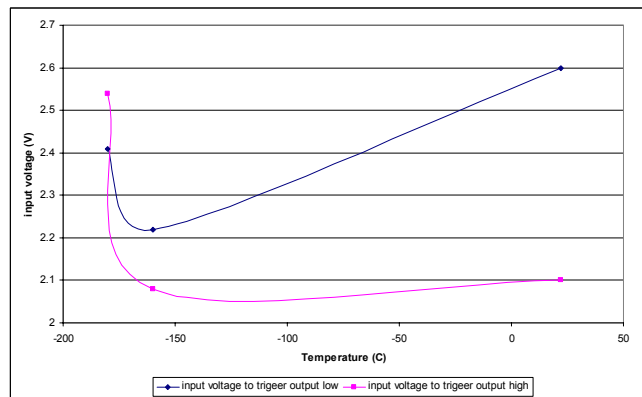

Figure 47. Input voltage to trigger output high and output low as a function of temperature.

Fuse

Three R459.250 (250mA) and three R451015 (15A) fuses were tested by using current probe Tektronix TM501, curve tracer Tektronix 576 and Oscilloscope Tektronix TDS744A.

One 5A fuse blew at 15.05A at 22ºC. 25A circuit breaker tripped on the curve tracer before the two 5A fuses blew at -160ºC and -180ºC. The 250mA fuses blew at 220mA at 22ºC, 300mA at -160ºC, and 315mA at -180ºC.

7.2. Cold Long Term Testing

The following electronics parts were biased for 1000-hour at -155C:

National Semiconductor NPN Supermatch Pairs LM194
Vishay Siliconix Matched N-Channel Pairs U430
Semicoa Semiconductors PNP Transistor Match Pairs 2N3811
Power MOSFET International Rectifier IRHNJ57034 60V NMOS
Power MOSFET International Rectifier IRHNJ597034 60V PMOS
Power MOSFET International Rectifier IRHNA57260SE 200V NMOS
Power MOSFET International Rectifier IRHNA597260 200V PMOS
Current Regulator Diode Interfet J554

A total of three test boards were used. Figure 48 and 49 show the top view and bottom view of board A. Board B and C have exactly the same layout.

Transistor pairs LM194, U430 and 2N3811, as well as two custom SOI 0.35um technology transistor packages A and B, were included on the top side of each board. The bottom side of board had all power MOSFET devices.

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The 1000-hour cold soak test was performed within a cryogenic chamber at a constant -150ºC with temperature fluctuation of +/- 5ºC for a total of 1000 hours. All the test devices were characterized at time zero, before the cold test started. The cold test was stopped at 100, 300, 500, 750 and 1000 hour points for intermittent characterization. All characterization was performed at room temperature.
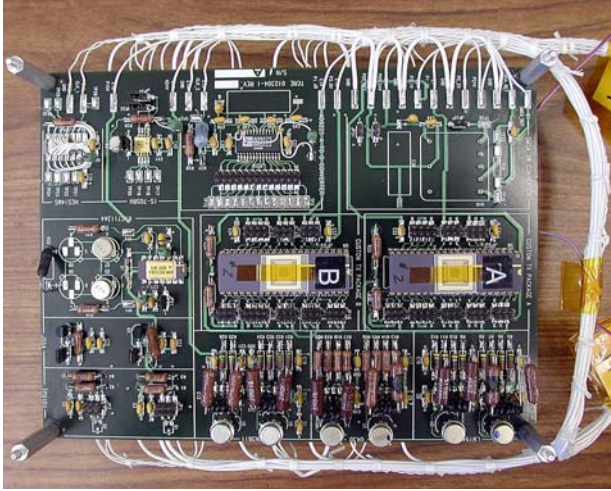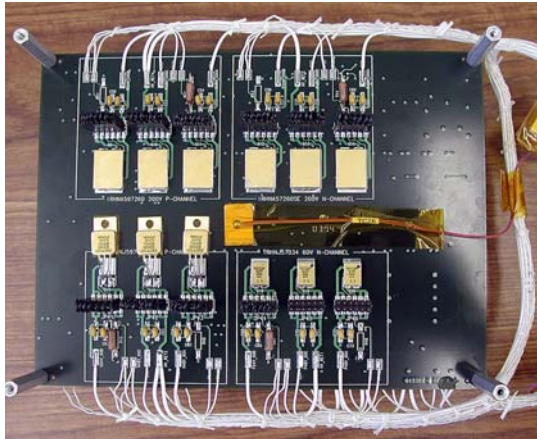

Figure 48. Top view of board A.

Figure 49. Bottom view of Board A.

LM194, U430, 2N3811

A total of six LM194, six U430 and six 2N3811 was biased during the 1000-hour cold test. A Keithley 4200 Semiconductor Characterization System was used to characterize the performance of the devices.

Two LM194 and two U430 devices failed due to ESD damage during the test, confirmed by failure analysis after testing.

LM194: Figure 50 shows the gummel plot for LM194 on board A as a representative curve. The DC gain change

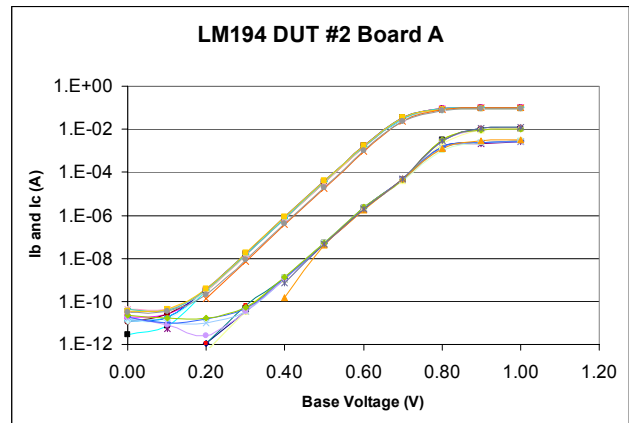when Vbe is from 0.3V to 0.7V is very small, but there is a shift when Vbe is greater than 0.7V.

Figure 50. Representative gummel plot for LM194.

U430: No noticeable degradation for U430 turn-off voltage when Vg<2.5V for devices on board. Turn-off voltage shifted less negative after the first 100 hrs for devices on board A, shown in Figure 51.
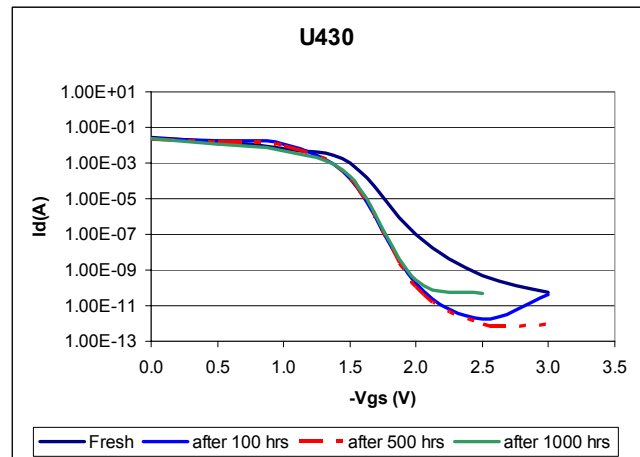

Figure 51. Turn-off voltage for U430.

2N3811: Shown in Figure 52, devices on board A started to have up to 1nA leakage current at low Vbe bias (less than 0.5V). No obvious degradation for devices on board B and C.
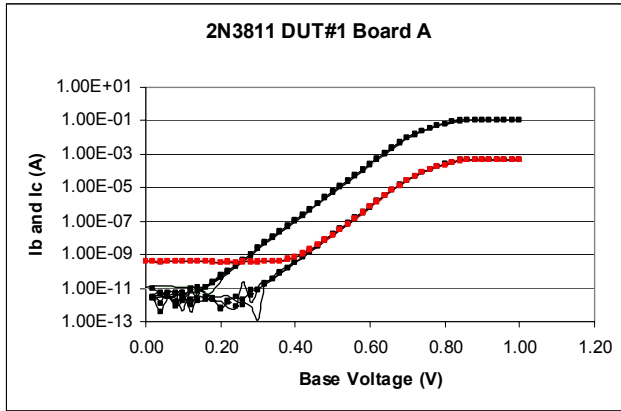
Figure 52. Representative gummel plot for 2N3811 on board A.

Power MOSFETs

A total of nine 60V Power nMOSFETs, nine 60V Power pMOSFETs, nine 200V Power nMOSFETs and nine 200V Power pMOSFETs were biased during the 1000-hour cold test. A Keithley 4200 Semiconductor Characterization System was used to characterize the performance of the devices.

60V nMOSFETs: Two of three nMOSFETs on board A, B and C failed after 100-hour cold soak. We suspect that the failures were induced by some board design issue(s), but it also could be due to the decrease of breakdown voltage under low temperature. Failure analysis on one of the 60V nMOSFETs showed possible ESD damage. For surviving 60V nMOSFETs, one on each board, there is no obvious degradation up to 1000-hour test.

60V pMOSFETs: There is no obvious degradation up to 1000-hour test.

200V nMOSFETs: There is no obvious degradation up to 1000-hour test.

200V pMOSFETs: All of three pMOSFETs on board C failed after 1000-hour cold soak. Failure analysis on one of the 200V pMOSFETs that the part was functional well and so the failure detected is suspected to be some interface failure/disconnection on the test board. For surviving 200V pMOSFETs, six total board A and B, there is no obvious degradation up to 1000-hour test.

J554

A total of six J554 was biased during the 1000-hour cold test, two on each board. All the J554 were tested to be failed on test boards after 1000-hour cold soak. However, all the parts were tested to be function after they were taken off the boards. Interface or disconnection on boards was speculated as failure source.

7.3. Design for Reliability

Design-for-reliability methodology was applied to a Quad Operational Amplifier circuit design for the wide temperature range application to ensure long term reliability. The Quad Op-Amp is shown in Figure 53. Hot carrier aging is the major intrinsic reliability concern at low temperatures; therefore, hot carrier tests were performed on the both NMOS and PMOS transistors from the SOI5 process at temperatures of -120 and -160ºC. It was observed that PMOS hot carrier aging lifetime was two orders of magnitude greater than NMOS lifetime; therefore, the minimum channel length determination was focused on NMOS only.
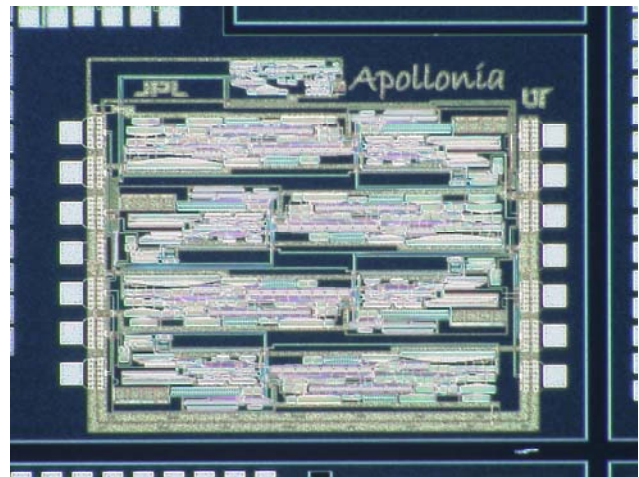

Figure 53: Quad Op-Amp

During hot carrier aging tests, the parametric characteristics, i.e,. saturation current I_{dsat}, linear current I_{dlin}, threshold voltage V_{th}, and transconductance g_m, were extracted from the I_{ds} versus V_{ds} and V_{gs} curves. Figures 1(a) and (b) show the change of *IV* curves during the hot carrier aging tests under $V_{ds} = 6.5$ V at -150ºC.

Figure 54 shows that hot carrier aging lifetime for 0.35um NMOS as a function of drain bias, with failure criterion defined as 10% maximum transcondance change based on QOA circuit requirements.
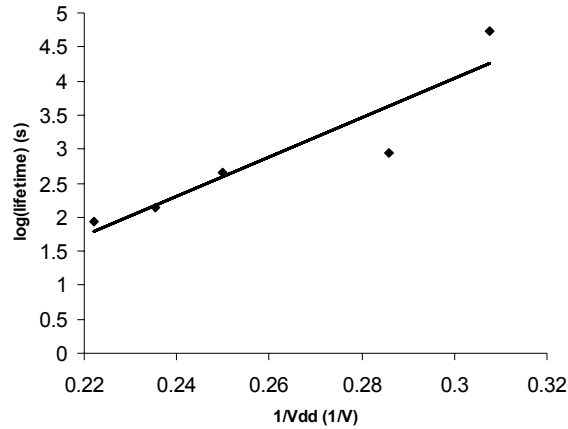
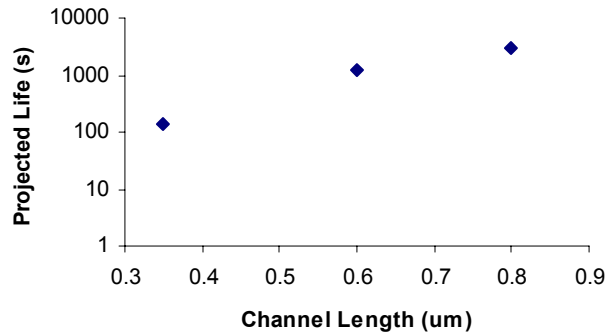Figure 54. 0.35um NMOS hot carrier aging lifetime at -160ºC.

Figure 55. Channel dependence of NMOS hot carrier aging lifetime at -160ºC.

In order to ensure a mission lifetime of 5 years minimum under the temperature range of -135 to 100ºC, a minimum channel length of the transistors inside the QOA is required. Based on the information from Figure 54 and 55, the minimum channel length was decided to be at least 0.9um for a 99.9% confidence level. The actual minimum NMOS transistor length used in the QOA circuit is 1.2um to ensure the target intrinsic reliability.

8. CONCLUSIONS

The survivability and reliability of selected electronics packaging assemblies and components were evaluated for integrated actuator and brushless motor drive electronics.

8.1 TCRE Packaging for integrated actuator and brushless

motor drive electronics packaging and components

For integrated actuator and brushless motor drive electronics packaging, the following results proved to find surviving materials for low temperature electronic packaging and understand the failure mechanism:

The TV1 failure analysis performed identified 5 different failure modes or types. All of these failure modes were related to the wire bond itself for all materials combinations. The failure or opens occurred at or near the wire bond peak, above the gold ball bond on the die side, above the gold wedge bond on the substrate side, at the gold wedge bond to substrate pad interface and at the gold ball bond to die pad interface.

Three dominant electrical failures occurred on TV2: 20 mil heavy Al wire bond lifting at the MOSFET die, nano-connector lead lifting, and R4 Sn62Pb36Ag2 endcap finish with In80Pb15Ag5 solder cracking. R1 and R2 with Sn90Pb10 and Ablebond 967-1 are still under investigation. Risk mitigation was applied to each failure. Material and process/assembly considerations were also made and mitigated for use in future experiments.

8.2 TCRE Electronics for integrated actuator and brushless

motor drive electronics packaging and components

For integrated actuator and brushless motor drive electronic components, we have identified, tested and characterized a group of COTS for operations over a temperature range of -135 to +125C. We also have developed a design-in reliability methodology for a quad operational amplifier that will be operated under low-temperature applications. In order to achieve the target reliability, the hot-carrier lifetime extrapolation model takes account of the evaluation of the hot carrier aging impact on the technology, analysis and simulation of circuit critical path and the determination of minimum channel length for critical transistors. This methodology can be applied to other electronics circuits operating with a varying low temperature ranges.

9. FUTURE WORK

9.1 TCRE Packaging for integrated actuator and brushless

motor drive electronics packaging and components

The risk mitigation of all electrical failures and material concerns and surviving material combinations will be applied to future test vehicles and implemented into the development of the universal motor drive electronics assembly. The continuous monitoring data will be analyzed in order to determine electrical failures that did not fail and should have failed based on the hypothesis. Finally, SEM analysis will be preformed in order to confirm the crack initiation in Sn phase on the lead finish and solder.

Several future experiments are also being pursued. For examples, the MOSFETs will be powered up during thermal cycling which will investigate the effect of the thermal stresses due to local heat rises of the device.

9.2 TCRE Electronics for integrated actuator and brushless motor drive electronics packaging and components

The future work include: 1) Large Sample Characterization of electronics parts for system level Worst Case analysis over temperature range of -135 to +125C. 2) Detailed performance and reliability characterization of the rad-hard qual operational amplifier for flight missions with a varying temperature range down to -135C.

ACKNOWLEDGEMENTS

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BIOGRAPHY

Carissa Tudryn began working at JPL in September 2004. She is a Mechanical Engineer in the Advanced Electronic Packaging Group. She has a Bachelor in Mechanical Engineering from The Catholic University of America and a Dual Masters in Mechanical Engineering and Materials Science and Engineering from the Massachusetts Institute of Technology.

Benjamin J. Blalock received his B.S. degree in electrical engineering from The University of Tennessee, Knoxville, in 1991 and the M.S. and Ph.D. degrees, also in electrical engineering, from the Georgia Institute of Technology, Atlanta, in 1993 and 1996 respectively. He is currently an Assistant Professor in the Department of Electrical and Computer Engineering at The University of Tennessee where he directs the Integrated Circuits and Systems

Laboratory (ICASL). His research focus there includes analog IC design for extreme environments (both wide temperature and radiation immune), multi-gate transistors and circuits on SOI, body-driven circuit techniques for ultra low-voltage analog, mixed-signal/mixed-voltage circuit design for systems-on-a-chip, and biomicroelectronics. Dr. Blalock has co-authored over 60 published refereed papers. He has also worked as an analog IC design consultant for Cypress Semiconductor Corp. and Concorde Microsystems Inc.

Dr. Gary Burke obtained his PhD in Computer Science in 1972 from Manchester University. Gary has been at JPL for 13 years, and is currently a Technical Group Supervisor in the Advanced Computer Systems and Technology group of JPL. Gary's main interest is advanced digital design, and he has been a Technical lead in many ASIC projects at JPL including CIA (Control ASIC), STM (transceiver), MCD3 (Viterbi Decoder), Block5 (Digital Receiver).

Yuan Chen received her Ph.D. degree in Reliability Engineering from the University of Maryland at College Park, Maryland in 1998, with a Graduate Fellowship from NIST. Now she is a Senior Engineer at Electronic Parts Engineering Office, Jet Propulsion Laboratory, Pasadena, CA and her work has been focused on the extreme environments technologies and development of reliability characterization and methodologies on microelectronic devices/circuits for space applications. Before joining JPL, she was a Member of Technical Staff at Bell Labs, Lucent Technologies from 1999 to 2002 and worked on device reliability, circuit and product reliability and qualification methodology. She is a senior IEEE member.

Scott Cozy has been at the Jet Propulsion Laboratory since 1997. He is a veteran of several robotic flight projects. The most notable being one of the designers of the Mars Exploration Rovers (MER) which landed on Mars in 2004. Prior to coming to JPL he received a Bachelors Degree in Computer Engineering / Computer Science from University of Southern California. While at USC he worked at the Robotics Research Laboratory and was responsible for the design and construction of 3 mobile robots (two wheeled, and one legged) and assisted with the Autonomous Flying Vehicle project. Scott was the recipient of NASA's Space Flight Awareness Launch Honoree Award in 2003 for his work on MER and has also received multiple NASA New Technology awards, primarily for innovative sensor

designs. His current work focuses on the Mars Science Lander Project scheduled to launch on 2009.

Dr. Reza Ghaffarian has 20 years of industrial and academic experience in mechanical, materials, and manufacturing process engineering. At JPL, Quality Assurance Section, he supports research and development activities in SMT, BGA, CSP, and MEMS/MOEMS technologies for infusion into NASA's missions. He was the recipient of NASA Exception Service Medal for outstanding leadership, industrial partnering, and expertise in failure modes and effects analysis and environmental testing of electronic packaging technologies. He has authored more than 100 technical papers, co-editor of a CSP book, 3 book chapters, two guidelines, and numerous patentable innovations. He serves as technical advisor/Committee to Chip Scale Review Magazine, Microelectronics Journal, SMTA, IMAPS, and IPC. He is a frequent speaker and chaired technical conferences including SMTA International, IMAPS, ASME, SAMPE, NEPCON, SEMI, IEEE CPMT, and IPC. He received his M.S. in 1979, Engineering Degree in 1980, and Ph.D. in 1982 in engineering from University of California at Los Angeles (UCLA).

Don J. Hunter is a Senior Member of the Technical Staff in the Electronic Packaging and Fabrication Section at Jet Propulsion Laboratory. He started at the Laboratory in 1993 as the lead Packaging Engineer for the Mars Pathfinder Mission. His major contributions include the development of a ruggedized 6U-VME-flight systems design. As part of the early X2000 Development Team, he received a Cal Tech and US Patent for work in advanced packaging systems architecture: Integrated 3D Technology on a Spacecraft Panel. As member of the Outer Planets Advanced Study Team, he has been involved in spacecraft system designs for future missions associated with the Comet Nucleus Sample Return and a Europa Lander. As a member of the Center for Integrated Space Microsystems Team his tasks have included the development of a technology test bed, feasibility studies for miniature science and navigation instruments, and activities pertaining to system-on-a-chip. He holds a B.S. in mechanical engineering from California State University Los Angeles and has been involved in the electro-mechanical packaging environment for over 23 years. He possesses experience ranging from commercial applications of deck top test equipment to military (DOD) cold temperature and high-G integrated packaging applications.

Michael Johnson has been with the Jet Propulsion Laboratory since 1986. He holds a Bachelor of Science in Mechanical Engineering and Physics. He is a licensed Professional Mechanical Engineer and is currently responsible for providing actuators for all of the Mars Science Laboratory mission applications. He has been

working on electro-mechanical actuators and their associated drive electronics since 1990. He also develops complete gyro-stabilized, multi-axis gimbal systems for the movie industry.

Elizabeth Kolawa has been with Jet Propulsion Laboratory (JPL), Pasadena, CA since 1993. Prior to joining JPL she was a Senior Research Associate at California Institute of Technology in Pasadena. Presently she is a manager of Extreme Environments and Space Avionics Technology program. Her current work focuses on the development of thermal cycle resistant electronics for Mars Science Laboratory as well as on extreme environment technologies for Solar System Exploration. Her research interests include electrical contacts to semiconductors, diffusion barriers, integration of Microsystems, sensors, and electrical packaging.

Mohammad Mojarradi received the Ph.D. degree in electrical engineering from the University of California, Los Angeles (UCLA) in 1986. Prior to joining Jet Propulsion Laboratory, Pasadena, CA, he was an Associate Professor at Washington State University and the Manager of the mixed-voltage/specialty integrated circuit group at the Xerox Microelectronics Center, El Segundo, CA. He is a Specialist in integrated mixed-signal/mixed-voltage electronic sensors, micromachined interface circuits, and mixed-mode integrated circuit design. He has more than 20 years of combined industrial and academic experience in his field. His current work focuses on developing highly efficient integrated mixed-signal electronics for sensors, actuators, and power management and distribution systems (PMAD) for avionics system on a chip for deep space using the SOI CMOS process.

Don Schatzel has been with the Jet Propulsion Laboratory since 2000. He is currently leading the Thermal Cycle Resistant Electronics team to develop advanced electronic packaging technologies for the Mars Technology program. He has over 20 years experience in electronics manufacturing and process engineering. He has worked as a Robotics Engineer for Motorola and as a Sr. Member Technical Staff, Project Manager, Manufacturing Operations Specialist and Six Sigma Blackbelt for Aerojet Electronic Systems. He is Group Supervisor for Advanced Electronic Packaging Engineering in the Electronic Packaging and Fabrication Section of JPL.

Andrew A. Shapiro has been working in microelectronic interconnects for twenty years. He has worked as a member of the technical staff at Rockwell International and Hughes Aircraft, where he was responsible for the packaging of a number of phased array radars and ran their high density interconnect line. He was a Principal Scientist at Newport Communications/Broadcom, where he made the first commercial polymer 10GHz Si packages. He has also designed and packaged 10 and 40GHz optoelectronic modules. He has also been Project Manager at California Institute of Technology's Jet Propulsion Laboratory and is currently a Principal Engineer in the Electronic Packaging and Fabrication Section (374) at JPL where he is implementing new electronic, RF and optical technologies onto space missions. He earned his BS in chemical engineering at U.C. Berkeley, his MS in Materials Science at UCLA and his Ph.D. in Materials Science at U.C. Irvine. He is on several national committees including NEMI optoelectronics roadmap, ECTC optoelectronics and, IMAPS education. Dr. Shapiro is also currently Assistant Adjunct Professor in Materials Science and Engineering at U.C. Irvine and is performing research in environmentally friendly manufacturing of electronics and optical and high frequency packaging.